SA-110 Microprocessor

Specification Update

July 1998

Notice: The SA-110 may contain design defects or errors known as errata. Characterized errata that may cause the SA-110's behavior to deviate from published specifications are documented in this specification update.

Order Number: 278104-001

Contents

Revision History

Date	Version	Description
06/15/98	001	This is the new Specification Update document. It contains all identified errata published prior to this date.
07/14/98	001	Product line order number sequence change, from 280104-001 to 278104-001. Under Affected Documents/Related Documents, changed order # to show change to Intel oder #.

Preface

As of July, 1996, Intel's Computing Enhancement Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order #
SA-110 Microprocessor Technical Reference Manual	278058

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Product Name product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	ERRATA
	S	#	#			
1	X			8	Fix	Potential Data Abort Occurs in Some Demand-Paged Memory-Management Schemes

Specification Changes

No.	Steppings		Page	Status	SPECIFICATION CHANGES
	#	#			
					None for this revision of this specification update.

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	#	#	#			
						None for this revision of this specification update.

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
				None for this revision of this specification update.

Identification Information

Markings

21281-AA, 21281-BA, 21281-CA, 21281-DA, and 21281-EA

- This document contains errata for the SA-110 Microprocessor. The SA-110 device revision that is affected by this errata can be identified as order numbers 21281-AA**,** 21281-BA**,** 21281-CA**,** 21281-DA**,** and 21281-EA.

Related Information

As of May 17, 1998, Digital Equipment Corporation's StrongARM, PCI Bridge, and Networking component businesses, along with the chip fabrication facility in Hudson, Massachusetts, were acquired by Intel Corporation. As a result of this transaction, certain references to web sites, telephone numbers, and fax numbers have changed in the documentation. Updates to this information are planned for the next version of this manual. Copies of documents that have an ordering number and are referenced in this document, or other Intel literature may be obtained by calling:

1-800-332-2717 or by visiting Intel's website for developers at:

http://developer.intel.com

The Intel Massachusetts Customer Technology Center services your StrongARM Product, Bridge Product, and Network Product technical inquiries. Please use the following information lines for support:

For Documentation and General Information	For Technical Support
Intel Massachusetts Information Line	**Intel Massachusetts Customer Technology Center**
United States:1–800–332–2717	Phone (U.S. and international):1–978–568–7474
Outside United States:1–303–675–2148	Fax:1–978–568–6698
Electronic mail address: techdoc@intel.com	Electronic mail address:techsup@intel.com

Errata

1. Potential Data Abort Occurs in Some Demand-Paged Memory-Management Schemes

Problem: There is an anomaly in the SA-110 device that may occur during a DATA_ABORT in environments that use demand-paged memory-management schemes. This problem has been seen only in demand-page memory-management operating systems when a memory access crosses a page boundary from a mapped page to an unmapped page during the sequence of data fetches.

Designs using operating systems with demand-page memory management schemes are susceptible to this problem. Designs using operating systems without demand-page memory management schemes, such as the following RTOSs, are not susceptible to this problem:

C-EXEC	Epoch32
Helios	Java OS
Kadak	Newton OS
Precise	pSOS
RTCX	Wind River

If you are not using one of the listed RTOS systems, you can check with your RTOS vendor to verify the method of memory-management scheme used to determine if your design is susceptible to this problem.

Implication: The Rn register may be incorrectly updated when a DATA_ABORT occurs during a load multiple registers, increment before (LDMIB) instruction. There is no known way to reliably replay the instruction after the data abort condition is corrected.

Problem conditions are:

1. The register list to be updated includes the base address register Rn.
   LDMIB Rn, {register list including Rn}
2. The LDMIB causes a data abort.
3. At least one register is loaded successfully prior to the abort.
   Rn = Rn + 4 (original value +4)

   If the abort occurs with no register loaded, Rn = Rn (the correct value).

If the instruction takes a DATA_ABORT after the first load completes successfully, the SA-110 incorrectly restores the base address register to base + 4. If the abort occurs immediately, the base address register is left at the correct value.

If a DATA_ABORT returns Rn with a value of Page_Boundary_Address (PBA) minus 4, it is unclear if the address is correct or if the correct address is PBA-8 with at least one register updated.

In actual operation, no code streams or data fetches are expected to DATA_ABORT at runtime (that is, any active process is fully mapped at runtime).

Workaround: None is required for operating systems that do not use demand-paged memory-mnagement schemes.

For operating systems that are susceptible to this problem, a revision of the SA-110 device intended to be fully backward-compatible and to correct this problem has been developed. The following table list the SA-110 devices and their old and new part numbers. The new parts are available now:

Device	Old Part Number	New Part Number
SA-110-110 MHz	21281-BA	21281-BB
SA-110-160 MHz	21281-AA	21281-AB
SA-110-166 MHz	21281-DA	21281-DB
SA-110-200 MHz	21281-CA	21281-CB
SA-110-233 MHz	21281-EA	21281-EB

Status: Fix. Refer to Summary Table of Changes to determine the affected stepping(s).

Specification Changes

None for this revision of this specification update.

Specification Clarifications

None for this revision of this specification update.

Documentation Changes

None for this revision of this specification update.