40-Gbit/s All-Optical Header Processing for Packet Routing[1]

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Abstract: We demonstrate 40-Gbit/s all-optical header processing using two ultrafast nonlinear interferometers to simultaneously forward two packets through a 2x2 spatial switch. Clear, open eye diagrams are observed, indicating low-error-rate fowarding decisions for packet routing.

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1. Introduction

In order to transmit packets from source to destination in telecommunication networks, the packet header must be processed at each router node before a forwarding decision can be made. Traditional electronic header processing requires demultiplexing to lower data rates followed by optical-electronic-optical (O/E/O) conversions for header separation and processing. As network channel data rates increase to 40 Gbit/s and beyond, faster header processing is required for minimizing packet processing latency and reducing congestion. One means of achieving high-speed header processing is to use optical signal processing techniques. Optical header separation and processing can be performed at aggregate channel data rates and offer decreased packet processing latency, short buffer lengths, payload transparency to bit rate and modulation format, fewer O/E/O conversions and a more straightforward switch structure requiring fewer input/output ports for the same bandwidth capacity. This results in reduced size, weight, and power requirements as compared with electronic solutions.

Previous optical header processing demonstrations have focused on keyword address recognition for broadcast-and-select networks [1-4]. For more general network topologies, we experimentally demonstrate a 40-Gbit/s optical header processor which can make simultaneous forwarding decisions for two packets propagating through a 2x2 electro-optic spatial switch. Our optical logic decision provides the capability for resolving contentions by giving priority to the packet desiring the cross state in the 2x2 spatial switch. For the ultrafast packet routing architecture described previously by our group [5], this header processing approach also provides unlimited address space and scalability with logic density that grows as $N \log N$ with port count N.

2. System Description and Results

The operation of the optical header processing unit for forwarding decisions in a spatial switching matrix is illustrated in Figure 1. In the Banyan switch matrix, only the jth address bit is needed to forward packets through the jth column in the switch matrix. Thus, header processing for two packets propagating through a single 2x2 spatial switching element requires only one address bit for each packet. As two optical packets enter a 2x2 spatial switching element, the header processing unit detects the "Empty/Full" bit and the address bit associated with each packet. This "Empty/Full" bit indicates the absence or presence of the payload in a packet. The header processing unit then configures a 2x2 switching element according to the destination address for a "Full" packet while ignoring the destination address of an "Empty" packet. When both packets are "Empty", we consider an arbitrary result to be acceptable. When both packets are "Full" and have non-conflicting destination addresses, either packet address will suffice. When both packets are "Full" and have conflicting destination addresses, we prioritize one packet over the other and thus allow for contention resolution to be implemented elsewhere in the network. One Boolean logic function which achieves this header processor operation is $R = E_1 \cdot A_1 + E_2 \cdot \bar{A}_2$, where R indicates the state of the 2x2 switch ("0"=bar, "1"=cross) and E_i and A_i are the "Empty/Full" bit and the address bit for the packet on input port i, respectively. If

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either "Empty/Full" bit is "0" ("Empty"), the corresponding address is ignored. If the "Empty/Full" bit is "1" ("Full"), the state of the 2x2 spatial switch is either set by the address of packet 1 or the inverse of the address of packet 2. Since the two packets arrive on different input ports of the 2x2 spatial switch, opposite switch states will forward each packet to the same output address. If both packets are "Empty", the switch remains in the bar state. If both packets are "Full", this logic prioritizes the packet requesting a cross state in the switch.

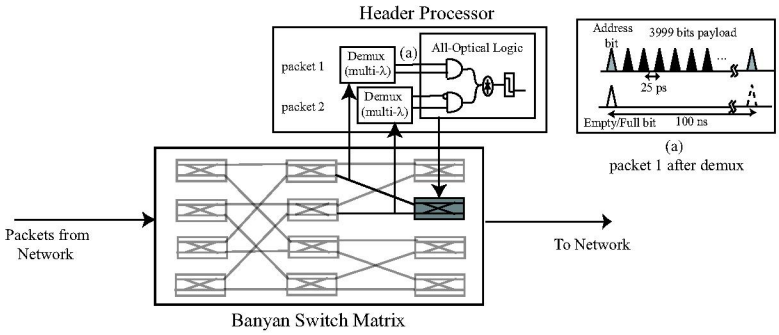

Fig. 1: Packet switching architecture

We demonstrate optical header processing after the detection or generation of the "Empty/Full" bit onto an intermediate wavelength. This can be achieved, for example, by using a single optical logic gate as demonstrated in [6]. In Figure 2 we show the experimental setup for the 40-Gbit/s packet generator, "Empty/Full" bit generator, header processor, and spatial 2x2 switch. The packet generator creates the address and payload by using a modelocked fiber laser to produce 2-ps pulses at 1547.5 nm modulated at 10 Gbit/s with a 2^7-1 pseudo-random bit sequence and optically multiplexed to 40 Gbit/s. The "Empty/Full" bits are created using a second, synchronized modelocked fiber laser generating 2-ps pulses at 1552 nm modulated with a "1001" pattern at 10 MHz. A diagram of our packet structure is shown in inset (a) of Figure 1. Two distinct packets are generated by introducing a 100-ns packet delay between the packet 1 and packet 2 channels. A similar delay between the two "Empty/Full" bits corresponding to the two packets produces a repeating pattern "10", "00", "01", "11". This explores all possible combinations of "Empty/Full" bits for the two packets. Furthermore, since the address bits of the two packets are created using a 2^7-1 pseudo-random bit sequence, all possible combinations of address bits for the two packets are generated.

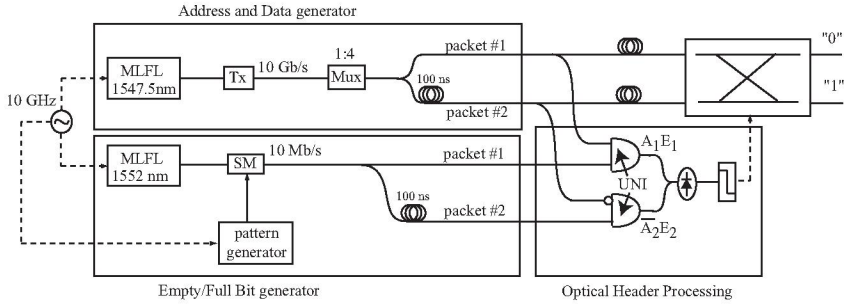

Fig. 2: System diagram of header processing and switching element for two packets

In order to implement the Boolean logic required to make packet forwarding decisions, two ultrafast nonlinear interferometers (UNI) [7], operating in co-propagating mode, are configured as AND gates with coupled outputs providing OR functionality. A signal pulse sent into a UNI is split into two temporally-delayed copies. A control pulse induces a π-phase shift in one signal pulse through cross-gain and cross-phase modulation in a semiconductor optical amplifier. When the signal pulses are recombined, the π-phase shift causes either destructive interference (inverting) or constructive interference (non-inverting). Thus, a UNI gate implements the logical functions of either $O = S \cdot \bar{C}$ (inverting) or $O = S \cdot C$ (non-inverting), where O is the output of the UNI, S is the signal input to the UNI, and C is the control input to the UNI. To generate $E_2 \cdot \bar{A}_2$, we use an inverting UNI gate with the address bit of packet 2 as the control input and the "Empty/Full" bit as the signal input. For packet 1, we use a non-inverting

UNI gate with the "Empty/Full" bit as the control input and the address bit as the signal input. Combining the outputs of the two UNI gates using a passive optical coupler provides the desired Boolean OR logic. Since the control and signal inputs to the non-inverting UNI gate are reversed from those of the inverting UNI gate, the two UNI outputs are at different wavelengths and inteferometric effects at the combining point are reduced. Furthermore, we ensure the output pulses are temporally separated by a delay greater than the pulse width and less than the photodetector rise time. Eye diagrams showing the results of the optical logic performed by both the non-inverting and inverting UNI gates are shown in Figure 3(a) and (b). These diagrams were taken with packet data rates of 40 Gbit/s and show a clear eye opening which can be used to achieve low-error packet-forwarding decisions.

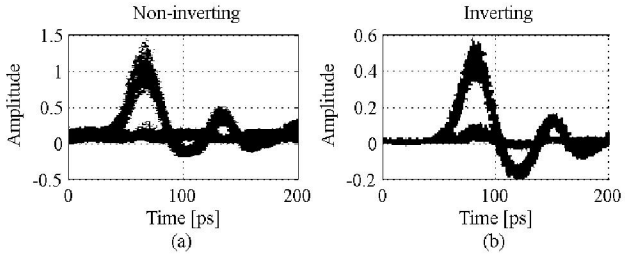

Fig. 3: Eye diagram of the co-propagating (a) non-inverting UNI and (b) inverting UNI used as header processing logic gates

The 2x2 spatial switch is implemented using an electro-optic lithium niobate modulator, which provides fast switching times and low crosstalk. To control this switch, the output from the header processor must be converted to an electronic pulse which is temporally matched to the packet duration. To perform this conversion, we use a high-speed 18-GHz photodetector followed by an 13-GHz electronic D-flip-flop. The packet processing latency of the optical header processing block is currently dominated by the fiber propagation times in the UNI gates. However, monolithically integrated optical logic gates can reduce the total packet processing time to below 1 ns. The switching time for the 2x2 electro-optic spatial switch is measured to be less than 1 ns. When combined with an integrated ultrafast optical header processor, only a 1-ns guard band will be required between adjacent packets in an ultrafast optical router [5]. The extinction ratio of the 2x2 electro-optic switch is measured to be >25 dB, which indicates that low interchannel crosstalk can be achieved between packets transmitted in parallel through both ports.

3. Summary

All-optical header processing can reduce packet processing latency and congestion in ultrafast routers as network channel data rates increase to 40 Gbit/s and beyond. Here, we demonstrate 40-Gbit/s all-optical header processing using two ultrafast nonlinear interferometers to simultaneously forward two packets through a 2x2 spatial switch. Clear, open eye diagrams are observed, indicating low-error-rate fowarding decisions for packet routing. This all-optical header processing design has the potential for sub-nanosecond latency with monolithic integration of the optical logic gates. Furthermore, the optical header processor also provides the capability for implementing contention resolution.

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