ANNUAL REPORT 2000

REALIZE THE ROADMAP

INTERNATIONAL SEMATECH

executive letter

Executive letter

(**above L-R**)
Dave Saathoff,
Chief Administrative Officer
Mark Melliar-Smith,
President and
Chief Executive Officer
Rinn Cleavelin,
Chief Operating Officer

2000 was a year of celebration. With the full membership of Hyundai, Infineon, Philips, STMicroelectronics, and TSMC, we became one global consortium, made up of thirteen companies representing Asia, Europe, and the United States, dedicated to cooperative efforts to improve semiconductor manufacturing technology. More than ever, our diversity is our strength. Unified by a common mission and governed by consensus, International SEMATECH (ISMT) represents a unique and rich blend of corporate and regional cultures. New perspectives, ideas, and approaches continue to broaden our capabilities, refine our processes, and generate successful results for our members.

2000 was a year of renewed commitment, as "Realize the Roadmap" became our prime directive. During the strategic planning process our Board of Directors and Executive Steering Council defined International SEMATECH's mandate to realize the Roadmap in six key focus areas: post-193 nm lithography, 193 nm optical extension, mask cost and availability, low-k materials, future gate stack, and manufacturing effectiveness. Our mission is to focus on critical technical challenges specified in the *International Technology Roadmap for Semiconductors* in these six key areas. We will accomplish this mission by concentrating on those programs best done in a pre-competitive consortium environment, delivering our programs when our members need them to stay on the Roadmap, and cooperating with and leveraging other sources of R&D for the benefit of our members.

We have undertaken the mission enthusiastically. It is not a radical departure from our continuing efforts through the years to help our members stay on the productivity curve defined by Moore's Law. Yet its importance today is even more crucial, as the technology and business challenges facing the industry grow in number, complexity, and urgency, and as the semiconductor industry plays a larger and larger role in fueling the global economy. Our successes in 2000 speak to our commitment to the following:

- **Focusing our technology programs on ISMT's core competencies, on what we can do best in each of the six key areas**
- **Partnering with suppliers, consortia, research institutes, and universities around the world to complement our programs and address industry-wide gaps**
- **Influencing the direction of the industry and its infrastructure by promoting the free exchange of ideas and best practices, and forging industry consensus**
- **Playing our part in keeping the semiconductor industry, and the global economy that it drives, strong and vibrant**

2000 was a year of achievement. The pages that follow chronicle ISMT's technical program results and highlight the value received by our member companies, the contributions of our assignees, various innovations in our support services, and activities that support our community. We would like to thank our member companies, our advisory boards, our worldwide partners, our local community, and particularly our own employees and assignees for making these achievements possible. We are proud of our efforts, but we are even more proud of the thirteen member companies we serve—for their successes in the marketplace, their commitment to pre-competitive cooperation, and the leadership they exert in the industry and in the world.

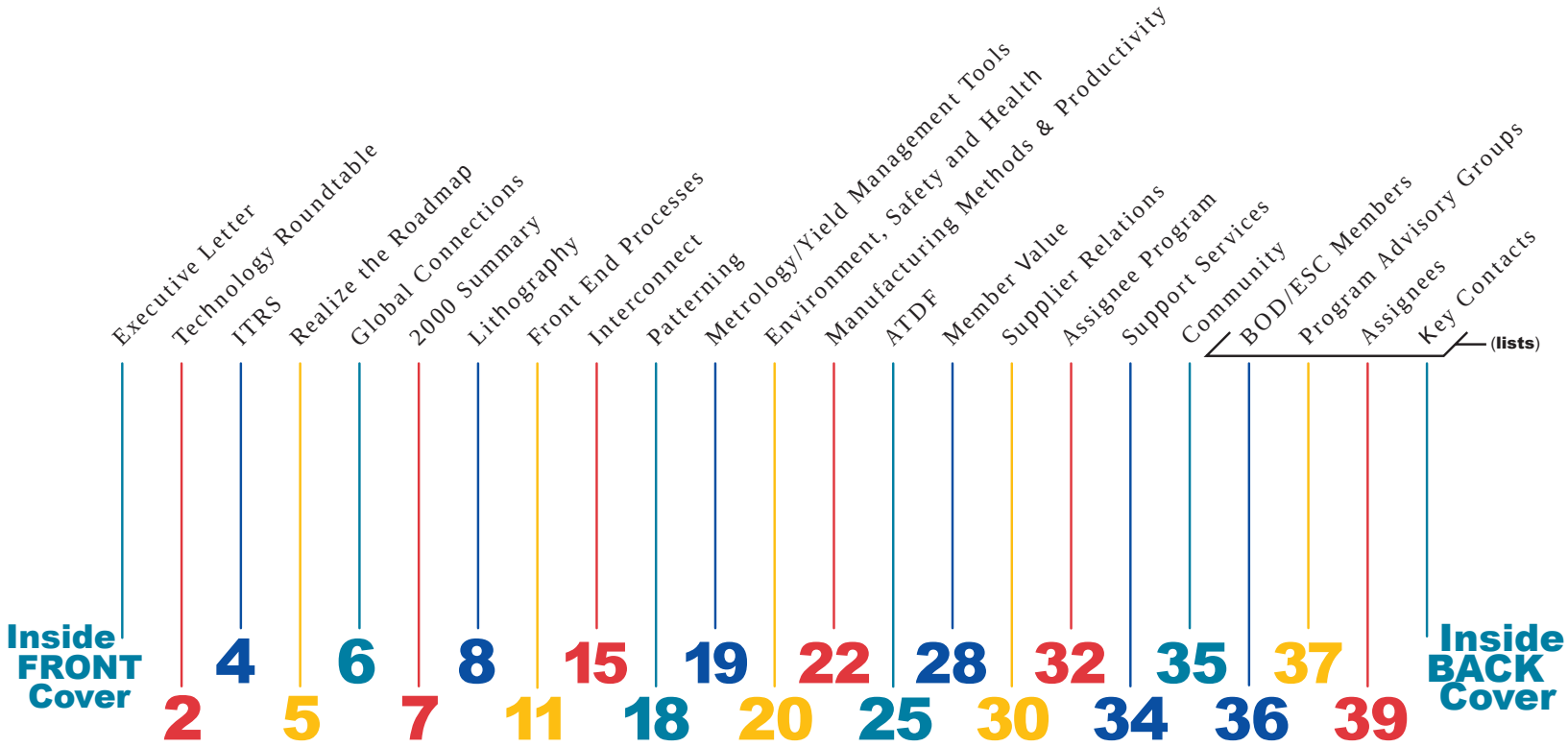
Mark Melliar-Smith
President and Chief Executive Officer

Rinn Cleavelin
Chief Operating Officer

David Saathoff
Chief Administrative Officer

AMD · HEWLETT PACKARD · IBM · intel · MOTOROLA · PHILIPS · TEXAS INSTRUMENTS · tsmc · CONEXANT · YUNDAI · Infineon technologies · Lucent Technologies Bell Labs Innovations

INTERNATIONAL SEMATECH



Mission

The members of International SEMATECH will gain manufacturing advantage through cooperative work on semiconductor manufacturing technology.

Vision

International SEMATECH is the most effective, global consortium influencing semiconductor industry directions and member company capability.

Values

Customer Focus
Technical Excellence
Quality Results
Accountability
Integrity
Open Communication
Safety
Teamwork

roundtable

Technology Roundtable: a Conversation with ISMT Technologists

With the increasing demand for portable electronic devices, and the continual push of Moore's law to quadruple the number of transistors on a chip every three years, CMOS scaling is being severely challenged in the drive to the 30 nm technology generation. Several of the leading technologists working at International SEMATECH (ISMT) recently discussed in a roundtable session the limits of—and likely replacement for—CMOS technology.

Peter Zeitzoff, Fellow: Conventional scaling is going to get very tough around the sub-50 nm generation, and certainly beyond that. MOS type devices will likely replace conventional planar CMOS, but they will be somewhat different structures. One of the devices under consideration these days is dual gate SOI or wraparound or vertical gate, which is probably do-able by similar processing techniques and tools that we have today.

Howard Huff, Senior Fellow: It appears that device fabrication down to approximately 15-20 nm channel length may be possible by utilizing the full suite of alternative MOSFET device configurations, which not only includes the vertical gate transistor that Peter referred to, but also the elevated source/drain, drain only, FinFET, ballistic transistor and additional alternative device configurations.

Ken Monnig, Associate Director, Interconnect: The Moore's law model has been predicated on planar MOS. It was planar PMOS for a while, and planar NMOS for a while, and planar CMOS for a while. Through all of that, we've been essentially gaining our performance by shrinking and not really doing too much to the device or to the processes. Now we are getting to the point where we are running into fundamental material limits and, yes, we can move to three dimensional devices to get us one more step on the Moore's law curve. And then we can move to optical interchip communication to get us one more step on the Moore's law curvestep. So each successive step on the Moore's law curve becomes increasingly more difficult, and the main question you have to ask yourself is: Are we ever going to get the return on the investment that you made to make that step? And that is, in some sense, not a technical question.

So, the question is: can we implement those solutions in a timely fashion, at a reasonable cost, and how many more generations on this sort of Moore's law performance versus dollar curve does that implementation buy you? Copper and low-k interlevel dielectric are another one of those things that, when you look at it, if you don't do anything else, if you do conventional scaling, you get one or two more generations out of it.

John Canning, NGL Program Manager: Lithography has been a key technology driver of smaller and faster devices. Extensions of optical lithography—by shorter wavelengths, higher numerical apertures, off-axis illumination, improved resist processes, and phase shifting masks—have driven the Roadmap on a two-year cycle down to the 100 nm node and possibly to 70 nm. Next Generation Lithography, such as EUV and EPL, holds the promise to go to 25 nm. A major concern is the economics: Will the cost-of-ownership be affordable, and can the mask industry fund the required R&D?

Another concern is the availability of interconnect materials with a resistivity lower than copper.

Monnig: If you continue to do conventional scaling, the Roadmap tells you to stay on the current performance curves, then yes, you would have to come up with another material by the 70 nm node, maybe 35 nm.

Canning: By what node?

Monnig: It depends on how far you think you can really push the dielectric constant, because there are really two materials at play here. There aren't any other materials in the periodic table that are lower resistivity than copper, except silver, and it's only about 10 percent less. It's not a technology generation's worth of less. So then what do you do? You could cool the devices, but that's a really big step. And when you look at that, you can squeeze maybe another generation or two out of it.

Zeitzoff: With the interconnect, you really hit the material limits that Ken mentioned very fast. But, in fact, the performance of ICs has ▶

(**below L-R**)
Alain Diebold, Senior Fellow
John Canning, NGL Program Manager
Ken Monnig, Associate Director, Interconnect



continued to improve rapidly because circuit designers have utilized clever and innovative circuit and architectural techniques to move around some of these apparent limits.

Huff: A system-level approach may indeed offer significant insight into those materials and process changes that will ultimately affect the device performance as observed at the consumer level.

Alain Diebold, Senior Fellow: In addition to worrying about the resistivity of copper lines when they get really thin, we are also concerned that more and more of the devices you want to make are for lower power than laptops—handhelds. You want the battery in your camera to last forever. Right now many of the things in the handhelds aren't quite at the technology edge, but they'll get there sooner and sooner as you want your telephone to be your PC.

Many other proposed technical advances will change our future. The lightweight, plastic display that can show a newspaper or a book, and then be folded and put in your pocket is one that fascinates me. We would have to have thin film transistors and liquid crystal or whatever kind of display technology built into it. You could imagine reading the newspaper one minute and be talking on the telephone to your kids the next minute with this device. All of those things drive totally different kinds of chips than we have considered in the past.

Zeitzoff: Your MOSFET device problems get complicated very quickly by going to very low power. You can tolerate pretty thin oxide-based gate dielectrics— (down to almost 1.0 nm) —where the total device leakage limits are relatively high, and hence, the gate leakage can be relatively high. But when you go to a very low power application where the total device leakage must be very low, then the gate leakage must also be quite low. To achieve such a low gate leakage requires a thicker (typically > 1.5 nm) gate oxide, but this thicker oxide usually results in poorer MOSFET device performance. To both control the gate leakage and to get high device performance, a high-k gate dielectric can be used. Timely availability of production-worthy high-k gate technology is being actively pursued.

Huff: In addition to more power-tolerant chip architecture IC designs, we might also apply more sophisticated power management schemes.

Walter Worth, Fellow: Another challenge that comes along with the shrinking of design rules is the accelerating pace of introduction of low-k interlevel dielectrics and the active developmental work in high-k gate dielectrics. There are new metal-based oxides, organic and siloxane compounds, as well as a variety of exotic CVD precursors. It becomes a real challenge for the industry to receive the necessary ESH data for these materials in step with the timeline for development of the new processes and tools, and their introduction into manufacturing. These ESH data are essential to identify any potential hazards early enough to switch to alternatives or to design in cost-effective administrative and equipment controls to protect the factory personnel and the environment.

Huff: Another important discussion that has been taking place in conjunction with the *International Technology Roadmap for Semiconductors* [ITRS] involves 450 mm wafers. As we are now entering the 300 mm wafer era, we are already hearing indications that 450 mm wafers may be necessary. Today, 450 mm is but a metaphor for a major productivity enhancement required by the industry to stay on our present business and economic growth trend. An actual wafer diameter change to 450 mm, however, will be needed if no other new productivity improvements are available, and these wafer size changes are always fraught with both economic and technical issues. Continuing to maintain a two-year technology cycle, as tactically envisioned in the ITRS, provides partial mitigation of the need for the next wafer size change, potentially delaying it on nearly a year-by-year basis. Assessment of these high-level ITRS strategies should be possible using the industry economic and productivity models presently under development at ISMT. ■



(**below L-R**)
Howard Huff, Senior Fellow
Walter Worth, Fellow
Peter Zeitzoff, Senior Fellow

itrs

Providing Resources and Direction

(**above L-R**)
Linda Wilson, ITRS Information Manager
Sarah Mangum, ITRS Webmaster

Before SEMATECH began operations, chip manufacturers, equipment and materials suppliers, national research labs, and university researchers gathered to set the charter for the new consortium. Known as roadmapping working groups, these teams created the blueprint for the consortium that would eventually become recognized as world class. The roadmapping that defined SEMATECH's operating plan resulted in another collective effort that would ultimately set the path for the entire semiconductor industry: a commitment to publish the first U.S. national semiconductor industry Roadmap in 1992. SEMATECH provided key technical support for this national roadmap and served as publisher of the document. Eight years later, International SEMATECH (ISMT) remains a key partner in this very important worldwide effort, known as the *International Technology Roadmap for Semiconductors* or ITRS.

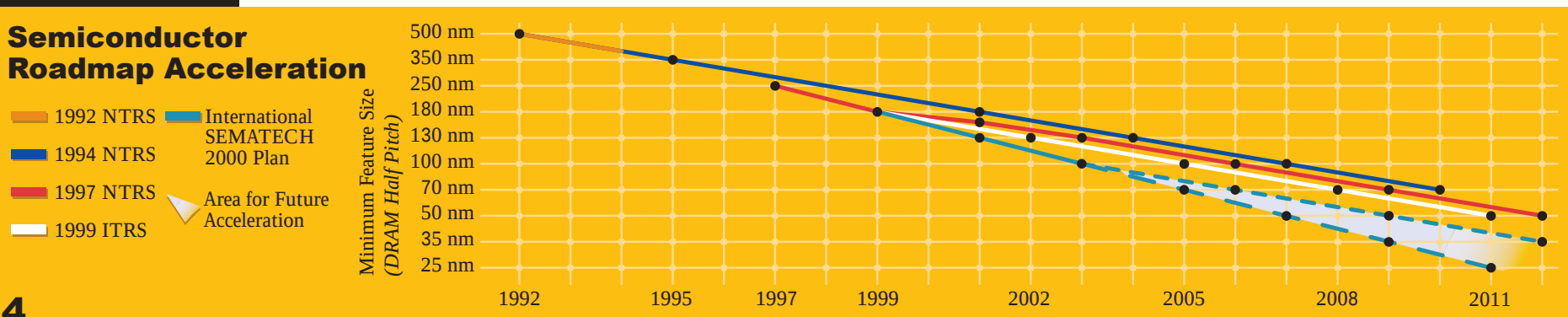
ISMT is involved in the ITRS at every stage of the roadmapping effort. The chair of the ITRS, Paolo Gargini of Intel, is a member of ISMT's Executive Steering Council (ESC), as is Fred Roosmalen of Philips, one of the European representatives on the International Roadmap Committee (IRC). Moreover, six of the twelve ITRS Working Group co-chairs in 2000 represented ISMT's efforts in Lithography, Metrology, Defect Reduction, Process Integration, Front End Processes, and Interconnect. In addition to those six Working Groups, ISMT technical experts actively participate in several other International Technology Working Groups (ITWGs). Representatives from ISMT's Interconnect, Front End Processes, Lithography, and Manufacturing Methods and Productivity divisions were also directly involved in the review or update of the overall Roadmap technology characteristics data for 2000 as part of the Chip Size Study Group task force.

During 2000, International SEMATECH's ITRS department coordinated several activities for the 2000 ITRS Update including continued management of the ITRS website, consulting and management of the April ITWG/IRC meeting hosted by the European IRC members in Leuven, Belgium at IMEC, hosting the annual ITRS summer conference in San Francisco, and consulting and support for the Taiwan-hosted ITRS conference in HsinChu, Taiwan.

ISMT published updated tables from each Working Group for the 2000 ITRS Update, coordinated all international communications among Working Groups, and posted all conference information and drafts to the ITRS website. The result of the year-long effort: on-time worldwide delivery of the on-line 2000 ITRS Update.

International SEMATECH's hands-on involvement in the ITRS gives member companies a preview of the 15-year assessment of industry technology, helping them to stay on the productivity curve. Through active participation in the ITRS Working Groups, ISMT member companies help define the potential solutions to key challenges, such as gate stack materials, mask cost, novel device structures and metrology at sub-70 nm. Member companies also gain exposure to manufacturers, suppliers, consortia, and academics from around the world. These relationships help foster the informal learning and exchange of pre-competitive technical expertise that helps our members realize the technological Roadmap. ■

(**below**)
ISMT implementation of the Roadmap with acceleration for members and suppliers beginning in 2003 as shown in the shaded portion.



roadmap

Realizing the Roadmap in Six Key Focus Areas

In the spring, the Board of Directors' Strategic Planning Subcommittee made a simple pronouncement on International SEMATECH's (ISMT's) strategic role over the next five years—"International SEMATECH," it said, "should help its members realize the Roadmap." The *International Technology Roadmap for Semiconductors* (ITRS) is a momentous plan for the industry to make itself 1,000 more times productive in fifteen years than it is today, and it is fraught with myriad technical challenges that must be overcome if the industry is to succeed. ISMT's role is to tackle those challenges, and to ensure that the materials, tools, and technology needed by the member companies to stay on the ITRS, or on their own internal roadmaps, will be available when they need them. According to OB Bilous, the consortium's new Chairman of the Board who led the strategic planning efforts, "The mission is not new; International SEMATECH has for years been working to keep its members on the historic productivity curve. But it has a new urgency. The industry is facing tremendous technology and business challenges more formidable and more complex than ever before. The prize for those who succeed in staying on the productivity curve will be continued growth and prosperity and failure for those who don't. It is clear to the Board that International SEMATECH must play a pivotal role in keeping the industry on track."

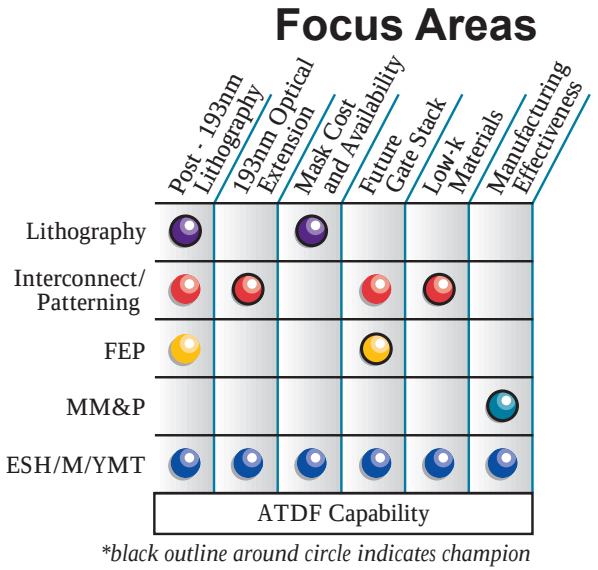
ISMT's senior technical advisors, the Executive Steering Council (ESC), concurred with the Board's "Realize the Roadmap" mandate, and further advised ISMT to focus its efforts on six critical Roadmap challenges in 2000-2001:

- Post-193 nm lithography
- 193 nm optical extension
- Mask cost and availability
- Future gate stack (with compatible ultra shallow junction)
- Low-k materials (k < 2.5)
- Manufacturing effectiveness

In each of these six key focus areas, the member companies affirmed that they look to ISMT to concentrate on programs best done in a consortium dedicated to pre-competitive cooperation—solving industry infrastructure issues, working on early materials efforts to reduce the number of potential options, working with suppliers on tool evaluation and improvement, and providing a single voice to the industry in areas such as economic modeling and standards.

In carrying out year 2000 programs, and particularly in developing annual plans for 2001, International SEMATECH launched a concerted effort to focus its resources on the six key areas. Division champions were identified, programs were designed and approved by the various advisory groups, partnerships were proposed and formed, and detailed 2001 project plans were solidly in place by year-end. Although ISMT remains a functional organization by technical divisions and enabling areas such as metrology/yield management, environment safety and health, and the Advanced Technology Development Facility (ATDF), the consortium has reorganized its efforts to focus on the few, most critical challenges identified by the members.

Focus areas will, of course, change over time; as technology challenges are met and overcome, new sets of challenges will take their place. International SEMATECH remains committed to concentrating programs on the issues most critical to the collective membership, and to delivering program results that "Realize the Roadmap" for its members. ■



**black outline around circle indicates champion*

(**above**)
International SEMATECH launched a concerted effort to focus resources on six key areas of wafer fabrication. Division champions were identified, and enabling areas provided needed support.

(**above**)
OB Bilous,
Chairman of the Board

connections

Expanding Global Connections, Forging Innovative Partnerships

The acceleration, increasing complexity, and rising costs of technology development in the industry make it clear that no company, nation, or region can hope to stay on the Roadmap without sharing the risks and rewards of technology research and development with global partners. Boundaries are disappearing, the members are engaging in growing numbers of alliances and joint ventures around the world, and International SEMATECH (ISMT) is nurturing its own network of global connections. To realize the Roadmap, ISMT continues to seek out world-class expertise wherever it resides to complement programs, bridge gaps in knowledge, and minimize duplication of effort.

Global membership and connections make ISMT an excellent catalyst for collaboration. Members look to ISMT to take the initiative in forming and managing partnerships with suppliers, consortia, research institutes, and universities worldwide, and ISMT takes pride in having put together a series of innovative and successful partnerships.

ISMT's Industry Executive Forums (IEF), led by Dave Anderson, director of Supplier Relations, bring together senior executives from the world's leading device manufacturers and equipment suppliers three times a year to discuss the business and economic issues facing the semiconductor industry, and how the two sectors can best cooperate to resolve them. The IEF discussions have spawned industry-wide cooperative initiatives such as Industry Economic Modeling, including academic research and the Global Economic Symposia/ Workshops, and ISMT's new e-Diagnostics program. A new focus in 2001 may lead to a set of projects jointly sponsored by chipmakers and suppliers aimed at resolving some of the key industry challenges at the interface of business and technology.

ISMT's relationships with Selete, a Japanese consortium, broadened and deepened during the course of 2000. Continued cooperation on a host of 300 mm-related projects, coordinated by Randy Goodall, MM&P associate director, and his team, led the way to new joint projects in the critical area of lithography masks, and, perhaps more significantly, to a series of Board-to-Board discussions on broader areas for future collaboration between the two consortia.

A long-standing relationship with the Semiconductor Research Corporation (SRC) continued to flourish, epitomized by the extension of the Front End Processes (FEP) Research Center for an additional two years. Under the leadership of Ed Strickland, External Research and International SEMATECH/SRC FEP Research Center program manager, the Research Center pools the talents of technologists from nine universities, the two consortia and their members, and equipment suppliers to discover solutions for the continued scaling of transistors.

In July, ISMT and IMEC, the Belgium-based research center, signed a joint research and development agreement to develop a new gate stack process for sub-100 nm semiconductor devices. This unprecedented multi-year, multi-million dollar international partnership represents a commitment to accelerate—by as much as two years—efforts to meet the ITRS gate stack/high-k requirements. Teams from both ISMT and IMEC worked long and hard through a series of complex issues to reach this agreement; for the first time ISMT assignees are working outside the United States.

A host of other cooperative projects with research labs, universities, consortia, and suppliers are also under way to realize the Roadmap: the standards program, under the direction of Jackie Ferrell, Guidelines and Standards program manager, continues to drive for industry consensus; work on equipment and process development continues with the Fraunhofer Institutes and with ASET; the ESH Division, represented by Jerry Chen, partners with universities in the Engineering Research Center for Environmentally Benign Semiconductor Manufacturing. Through all the various partnerships, ISMT works to keep its members and the industry on time, on target, together. ■

(**below L-R**)
Ed Strickland,
Program Manager,
External Research and
International
SEMATECH/SRC
FEP Research Center
Jackie Ferrell,
Program Manager,
Guidelines and Standards
Randy Goodall,
MM&P Associate Director
Jerry Chen,
Project Manager,
Water Optimization




2000 summary

Highlighting the Year's Accomplishments

Thanks to the vision, support, and direct involvement of the member companies, 2000 was a year of achievement for International SEMATECH (ISMT). Each of the technical divisions and support programs played a part in realizing the Roadmap, and each shared in ISMT'S overall success. The following pages of this annual report chronicle the details; here are a few highlights.

91% of Deliverables Met On Time

Even in the face of an ever-accelerating Roadmap, International SEMATECH's technical programs continued to progress well. 91 percent of the master deliverables were delivered to the members on schedule, the highest level ever achieved by the consortium, and 97 percent were completed by year-end.

157 nm Lithography

Through specific programs focused on the micro exposure tool and material development and testing, and through a series of global meetings designed to build consensus, ISMT has built enough confidence in 157 nm technology that the whole industry is now supporting the introduction of 157 nm at the 70 nm node. Members can be proud of the consortium's pioneering effort in laying the groundwork for this important technology.

Gate Stack and Ultra Shallow Junction

New gate stack materials and the ultra shallow junctions needed to extend planar CMOS beyond 70 nm were the focus in Front End Processes; an important achievement was the delivery to our members of the first set of transistor data using high-k dielectrics. Excellent progress was demonstrated on high-k materials, metal gate electrodes, and ultra fast annealing techniques.

Low-k Materials

Interconnect continued to offer significant value to members through its work on very low-k materials and very thin barrier layer technologies. Key to this success was the successful integration of a two-level dual Damascene process using a porous low-k dielectric.

e-Diagnostics

Ramped up at "Internet speed" this year at the request of ISMT's Board of Directors and the Industry Executive Forum, the e-Diagnostics program attracted industry-wide participation and made great strides in driving pre-competitive technology and open standards in this emerging field.

Metrology/Yield Management Tools Initiative

International SEMATECH and leading tool suppliers brought together an array of metrology and defect detection tools to spur the development and evaluation of new technologies to characterize masks, measure process variation, and ensure product quality.

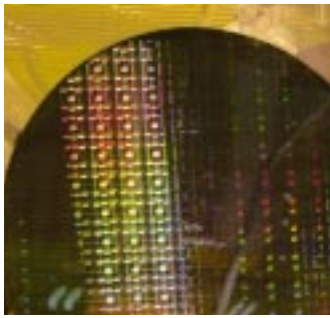
Resource Conservation

For a relatively small program, ESH packs a large punch, having been instrumental this year in initiatives to reduce water use and energy consumption in production facilities.

ATDF Cycle Time and 300 mm Support

Focusing on cycle time and customer satisfaction has improved the throughput of the Advanced Technology Development Facility (ATDF) by a factor of three. Moreover, member companies have benefited from the ATDF's increasing 300 mm support capability; this year the ATDF supplied over 7,000 300 mm wafers to member companies starting up their pilot lines, helping to accelerate the critical time window between tool acceptance and wafer starts.

ISMT's success in 2000 was broader than just these highlights. It involved a whole host of technical projects, as well as initiatives implemented by the various support services organizations to keep the consortium both effective and efficient. ISMT's achievements are a result of the dedication and hard work of many people—employees, assignees, member companies, and global partners—all working together to realize the Roadmap. ■



Lithography: Leading Technology Acceleration

(**above L-R**)
Rich Harbison,
157nm Program Manager
Gene Feit,
Resist Development
Manager

(**above L-R**)
Gerhard Gross,
Director of Lithography
Wally Carpenter,
Mask Strategy Program
Manager
John Canning,
NGL Program Manager

International SEMATECH (ISMT) continues to lead the development of future solutions for the rapid acceleration of the lithography technology nodes for the worldwide semiconductor industry. The acceleration of the technology nodes outlined in the *International Technology Roadmap for Semiconductors* (ITRS) provides opportunities—and poses challenges—to ISMT's role in guiding the industry in developing processes and materials leading to the manufacture of sub-100 nm devices. In 2000, International SEMATECH once again brought together global industry experts in various forums and symposia to unravel the complicated number of choices and challenges that must be overcome to reach a consensus on the direction of the next stage in lithography technology.

"We are providing strategic leadership for our member companies and for the industry," said Gerhard Gross, director of Lithography and an Infineon assignee. The work at International SEMATECH includes the support of suppliers and infrastructure development for all aspects of lithography so that member companies receive from their International SEMATECH membership a technology "package" that will meet their lithography needs. "What's a scanner without resist?" said Gross. "You need it all, and we investigate the entire lithography package. International SEMATECH is driving the development of the technology and infrastructure for future lithography."

Of the six key focus areas identified by the International SEMATECH Executive Steering Council (ESC), two—Post 193 nm Technology and Mask Cost and Availability—reside within the Lithography Division. Consequently, ISMT's advanced lithography work (Post 193 nm Technology) concentrates on two areas: pushing optical lithography, including 157 nm, to and possibly below the 70 nm node, and driving global consensus on Next-Generation Lithography (NGL) options and timing.

"In our 157 nm and NGL approaches we are leading the world. Our efforts have provided member companies with the first 157 nm evaluation tool," said Gross. The Exitech 157 nm microstepper installed in ISMT's fab is used by suppliers in the development of production-worthy resists. Gross adds that a planned insertion in 2003 of the EUV Micro Exposure Tool will provide member companies with a similar capability in today's mainstream NGL technology.

Timing in lithography is one of the major and most critical tasks that International SEMATECH is tackling for its members and the industry. "We are supporting the development of the infrastructure for the upcoming technologies in a shorter time period than we have ever faced before," said Gross. Key accomplishments and challenges within Lithography in 2000 helped to define more tightly the direction needed to deliver the technology on time, at the right node.

157 nm Lithography

Three years ago, 157 nm technology was not considered an option for the extension of optical lithography. Today, as a result of ISMT's work on behalf of its members and the industry, 157 nm technology will likely take the industry to the 70 nm node. "Because of International SEMATECH's technology leadership, there are few, if any, obstacles left to prevent 157 nm lithography from becoming a reality," said Rich Harbison, 157 nm program manager.

ISMT is working in each of these areas identified in the table below, often in conjunction with material suppliers. For example, the consortium and vendors are testing new pellicle materials that not only have the required transmission at 157 nm, but more importantly, ▶

Critical Issues Facing 157 nm Development
Reticle defect control
Resist capability for 100 nm (practical thickness)
Timing/risk of production tools for the 100 nm node
Calcium fluoride for lens materials
Contamination control of the optical path
Attenuated phase shift mask material
Cost of ownership

(**right**)
ISMT members ranked and identified key 157 nm challenges at the 157 nm technical data review in November.

also have sufficient resistance to high-energy radiation so that they do not darken after multiple exposures.

Resist

International SEMATECH took delivery in 2000 of the first 157 nm lithography microstepper from Exitech Ltd., and within weeks ISMT achieved performance levels equal to or better than those of its 193 nm microstepper. Without resorting to phase shift masks, 1:1 line and space patterns were resolved at 110 nm and 1:1.5 line and space patterns were achieved at 90 nm.

"This represents a tremendous boost to the continuing momentum of 157 nm technology," said Gene Feit, manager of Resist Development. ISMT plans to have prototype resist materials available by the end of 2001 and manufacturing quality material ready by the end of 2003. The microstepper is available for use by suppliers and member companies at ISMT's Resist Test Center (RTC) housed in the Advanced Technology Development Facility (ATDF). Significant progress has been made in developing new polymer backbones, which will provide sufficient transparency at 157 nm to allow reasonable resist thicknesses to be used for single layer resists. In addition, work continues on thin layer imaging and bi-level resists.

In 2Q 2000, 193 nm resist benchmarking was completed. The final report gave member companies a clear picture of both the state-of-the-art and areas in need of improvement. The 193 nm resist activities were transferred to the Patterning program at the end of 2000. Patterning will continue to extend current 193 nm technology further than technologists have historically thought possible.

Next Generation Lithography (NGL)

At the fourth NGL Workshop sponsored by International SEMATECH in September, the world's leading lithographers recommended that the worldwide industry narrow the NGL options to Extreme Ultra Violet (EUV) and Electron Projection Lithography (EPL).

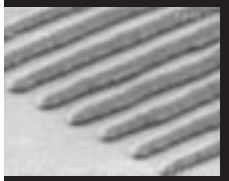
"International SEMATECH's workshop builds global industry consensus on the NGL options, and that becomes increasingly important as NGL technology moves out of the R&D arena into the supplier area, where the entire infrastructure for this new technology is created," said John Canning, NGL program manager. "Commercial equipment suppliers are increasing their involvement in NGL through prototype tools planned for completion as early as year-end 2003," said Canning. "However, there still remain fundamental critical issues that require increased R&D efforts before these two approaches can get the full industry go-ahead for insertion at the 70 nm node." ISMT is addressing those critical issues in EUV and EPL through 13 projects, ranging from defect-free EUV mask blanks and EPL mask manufacturing on thin membranes, to high NA optics manufacturing for the EUV Micro Exposure tool.

Mask Cost and Availability

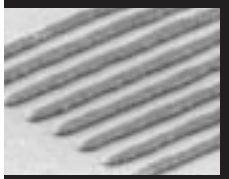
During the past decade, the ITRS has been continually accelerated as the industry has found ways to improve lithography faster than expected. Much of this improvement has come from the ability to use sub-wavelength imaging techniques, including optical proximity correction and phase shift masks. However, these techniques place an increasing demand on the masks themselves both in terms of feature sizes and in materials and process complexity. For example, the effect on CD uniformity has been most pronounced with the target specifications pulled in by as much as five years earlier than defined just two years ago. These challenges have resulted in lower yields, higher costs and unacceptably long mask manufacturing times. In addition, the advent of 157 nm exposure tools requires changes in the mask substrates and the phase shifting materials. To ameliorate these challenges, ISMT has initiated a number of active programs with mask processing tool vendors in the area of write, inspect and repair, programs designed to improve yield and throughput, and to handle the more aggressive plans for improved resolution and optical enhancement techniques.

"Our strategy is to mitigate the risk those challenges pose by evaluating the most significant options for our members and driving for ▶

(**above**)
Used for advanced optical lithography development in the Resist Test Center of International SEMATECH, the 157 nm Exitech Microstepper produces features < 100 nm.



(**above**)
110 nm 1:1 line and space patterns



(**above**)
90 nm 1:1.5 line and space patterns

timeline

Litho Highlights

Q1
• Delivery of the first 157 nm lithography microstepper from Exitech Ltd.

Q2
• 1st International Symposium on 157 nm Lithography held • 1:1 line and space patterns were resolved at 110 nm and 1:1.5 line and space patterns were achieved at 90 nm on the 157 nm microstepper • 193 nm resist benchmarking completed • 13 projects launched on EUV and EPL Critical issues • Alternating PSM inspection project launched

Q3
• Fourth NGL Workshop sponsored by International SEMATECH builds global consensus

Q4
• 157 nm Technical Data Review reprioritizes critical issue list

Electronic Voting Speeds Decision-Making

Over the last three years, International SEMATECH (ISMT) has used an electronic decision support system that allows for anonymous votes, real-time results, and sophisticated graphing and ranking that gives members a clear picture of critical projects and key issues. With projects as complex as those at ISMT, the ability to compare and rank various projects against one another is crucial in decision making.

"It's very important for International SEMATECH to understand what our thirteen member companies consider critical," said Walter J. Trybula, manager of Productivity and Support in Lithography. Although other ISMT divisions, such as ESH, use the decision support system, Lithography initiated and heavily employs its use at various technical workshops and advisory group meetings.

A major advantage of the system is the anonymity it allows participants. In the past, voters walked to the front of a meeting room and stuck adhesive dots onto paper flip charts that contained the various choices up for consideration. Because of cultural differences among member companies, some company representatives were uncomfortable with the public nature of their vote. "This decision support system permits everybody to have an equal but anonymous voice," said Trybula.

The system has been used in ISMT's Next Generation Lithography workshops and 157 nm meetings, as well as in the Lithography, ESH, and Patterning program advisory groups.

"We can cover a tremendous amount of material in a relatively short period of time. This process is at least six times faster than using the sticky dots," said Trybula.

Lithography (continued)

the most cost-effective solutions," said Wally Carpenter, Mask Strategy program manager and an IBM assignee.

According to Carpenter, new mask-making equipment—technologically ahead of the need—is required to get mask yields up. That effort drives very aggressive and potentially expensive equipment development programs. "That's where International SEMATECH plays a critical role, by subsidizing those equipment development costs and effectively 'buying time.' Equally important, through our programs International SEMATECH members provide suppliers with clear industry direction," he said. Major developments in 2001 will include the availability of the ETEC Mebes X write tool for 130 nm capability, the KLA DUV inspection tools, and the RAVE repair beta tool. With delivery expected by 4Q 2001, the RAVE mask repair tool will provide ISMT member companies with a new and innovative technology. "With these tools in place, we will be able to test the masks, inspect them and—equally critical—repair them if defects are found, at yields that will keep masks affordable," said Carpenter.

International SEMATECH is also working in collaboration with Selete, a Japanese consortium, to address mask handling infrastructure changes, both for mask-makers and inside production facilities. The steps required to bring 157 nm mask capability to the industry call for a global approach. ISMT and Selete are addressing mask issues through collaboration on blanks transmission, surface contamination, and electrostatic discharge (ESD).

Recent delays in delivery of crucial mask equipment have caused IC manufacturers to consider maskless lithography, and ISMT is exploring the benefits and drawbacks of such an approach. Maskless lithography will be added to the agenda of the fifth NGL workshop hosted by ISMT in August 2001. "We must have a back-up plan in the event that we are unable to overcome the challenges involved in using masks. We need a strategy that will bring us to the 50 nm node and below," said Gross. ■

(**below**)
Top preferences for technology nodes among NGL Workshop participants.

Narrowing the NGL Options	
130 nm	248 nm optical and 193 nm optical
100 nm	193 nm optical and 157 nm optical
70 nm	157 nm optical, and EPL and EUV
50 nm	EUV and EPL
35 nm	EUV

(**left**)
The key elements of the decision support system are the computer with the controlling program, a transceiver for receiving the radio signals, and the handhelds with a keypad for selection of a voting choice. The computer screen shows the ranking of project importance by compiling the individual votes cast. As the use of these tools becomes more widespread, additional features can be employed to increase the decision making support available to the member companies.

fep

Front End Processes: Focusing on the "Grand Challenge"

As semiconductor devices continue to shrink, the processes and materials used to make them are rapidly approaching their physical limits. To take full advantage of the reduced design rules of the *International Technology Roadmap for Semiconductors* (ITRS), the industry must move to thinner gate dielectrics for sub-70 nm devices. Silicon dioxide, which has been the heart of the MOS transistor for the last 40 years, is unable to perform to ITRS requirements at thicknesses at or below 1.5-2 nm because of excessive leakage and reliability problems. The ITRS calls for new dielectric materials to replace silicon dioxide; transistors using these high-k dielectrics are projected to enter manufacturing by 2005.

This year International SEMATECH (ISMT) delivered to its member companies the first set of transistor data using high-k dielectrics, a major step toward achieving a fully integrated high-k transistor. "This data puts our member companies and the industry on the right track in finding a replacement for current gate stack materials," said Mike Jackson, director of Front End Processes (FEP). "We're now in a position to make real life, conventional planar CMOS transistors using high-k materials. By bringing in suppliers at this stage, we will guide the industry to worldwide consensus for these new materials to ensure that we have ideal process equipment for manufacturing."

Among the topics covered in the report are the thermal stability of high-k materials, effective dielectric constant, leakage current, and integration. "We are moving away from something [SiO_2] that has been used for 40 years, and it's a real challenge," said Jackson. "How these materials behave when combined in conventional CMOS processes is one of the big questions that we are helping to answer," he said. For example, if annealed at too high a temperature, some materials lose their high-k characteristics. "Such integration issues," said Doping Program Manager Larry Larson, "represent the key challenge in manufacturing transistors of the future."

Newly Acquired Equipment Gives International SEMATECH Capability to Deposit Candidate High-k Materials

In the past, high-k development has been limited by the availability of deposition systems to produce the layers to be tested. This limitation has been overcome with the acquisition of the Applied Materials MOCVD chamber and an ASM ALCVD chamber. Moreover, ISMT will benchmark other tools and techniques in coordination with IMEC, the Belgium-based, government-supported research institute, and the Fraunhofer Institute. "Our strategy is to accelerate that movement from the research state right into production," said Jackson. "Having a flexible set of tools provides us with different techniques, so if IMEC or the FEP Research Center recommends an alternate material, we can test it for manufacturability."

100 nm Technology Ultra-Shallow Junctions Demonstrated

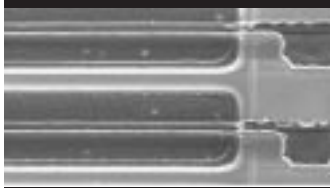
Using low energy ion implantation and spike annealing, ISMT has been able to get to 100 nm and 70 nm node requirements for ultra shallow junctions. The ITRS requires junctions of 250 Å for the 100 nm technology node. Due to an effect called transient enhanced diffusion, any implanted junction occurs at least at that depth when annealed. "The challenge involved in this is to discover implant and anneal techniques that can provide shallower junctions than allowed by this effect," said Larson. "It is important to realize that forming junctions and finding a high-k material system cannot happen independently. The most challenging of the issues facing FEP is delivery of ultra shallow junctions and high dielectric constant in the same manufacturing-worthy transistor flow."

Because it appears that implant and anneal techniques will not work at the 50 nm node, ISMT has begun a major activity looking at alternative methods of producing shallower junctions.

Gate-quality Silicon Nitride Benchmarked

Nitride-based dielectrics are used now as one of the primary dielectric systems in the manufacture of transistors, and will remain the system of choice until an acceptable, manufacturing-worthy high-k dielectric is developed. Consequently, benchmarking silicon nitride has immediate benefits to our member companies. A study conducted at the University of California at Los Angeles for International SEMATECH found that nitridation of a furnace or rapid thermal processed (RTP) silicon dioxide by remote plasma nitridation (RPN) is feasible. Compared to plasma-nitrided oxides, silicon nitride films deposited by rapid thermal chemical vapor deposition (RTCVD) have several drawbacks. These RTCVD nitride films ▶

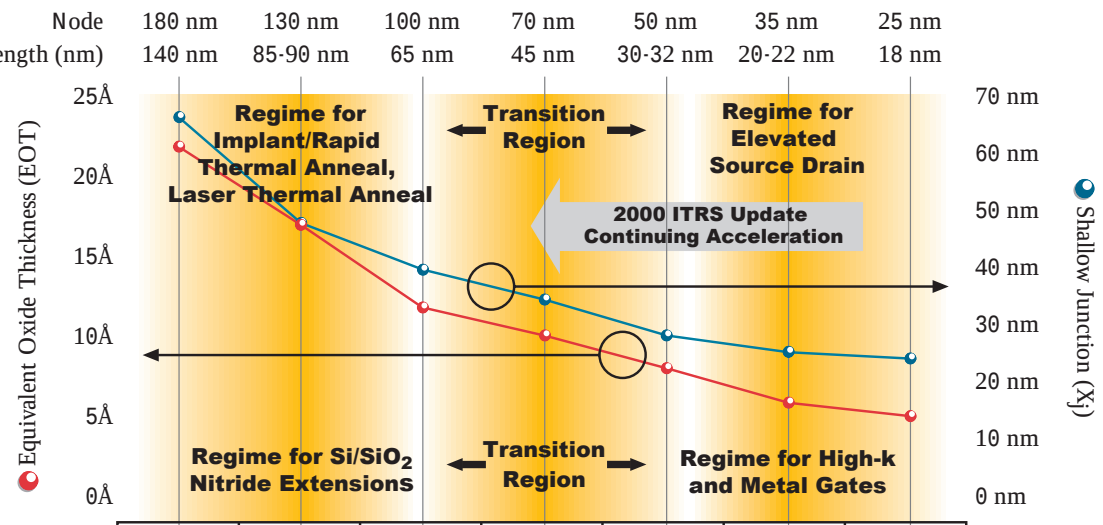
(**above L-R**)
Mike Jackson, FEP Director
Larry Larson,
Doping Program Manager



(**above L-R**)
International SEMATECH demonstrated the consortium's first working PMOS transistors with Laser Thermal Anneal (LTA) in August 2000.

Planar CMOS Grand Challenges

Based on the 1999 International Technology Roadmap for Semiconductors (ITRS)



	1999	2002	2005	2008	2011	2014	2017
EOT	22Å	17Å	12Å	10Å	8Å	6Å	5Å
Xj	66 nm	48 nm	40 nm	34 nm	28 nm	25 nm	24 nm

generally require multi-step processing—as many as four steps in the better-performing films—that can significantly reduce process throughput. In addition, there is generally a trade-off between the achievable equivalent oxide thickness and transistor mobility.

Plasma-nitrided oxides have exhibited an order of magnitude lower gate leakage current and comparable saturation current to pure oxides. Only a small degradation in device mobility—three percent for PMOSFETs and seven percent for NMOSFETs—with plasma-nitrided gate dielectrics has been observed. In contrast, RTCVD nitrides can lead to more than 50 percent degradation in transistor mobility for an equivalent oxide thickness (EOT) of approximately 1.4 nm. An EOT of about 1.4 nm has also been achieved using the RPN process. Mobility data on these films is currently being collected.

"People are really interested in high-k materials, but you don't need them today," said Jackson. "This work has helped delay the need for high-k materials to the 100 nm node or beyond."

100 nm Technology Modeling

In 2000, FEP established a modeling tool that both demonstrates 100 nm technology and allows discussions with suppliers and other ▶

timeline

FEP Highlights

Q1
- Benchmarked gate quality silicon nitride tools and techniques
- Key report on high-k dielectric material selection issued by the FEP-RC
- Benchmarked ultra-shallow junction high ramp rate spike anneals

Q2
- AMAT Centura upgrade with RPN capability
- ASM ALCVD high-k chamber installed
- Investigation of the effects of cleans on EOT and effects of carbon contamination on electrical performance/reliability completed and reports issued
- Established modeling tool that demonstrates 100 nm technology
- Demonstrated 100 nm technology node ultra-shallow junctions using Laser Thermal Annealing (LTA)
- Demonstrated 130 nm PMOS and NMOS capability on ultra shallow junctions in ATDF

FEP (continued)

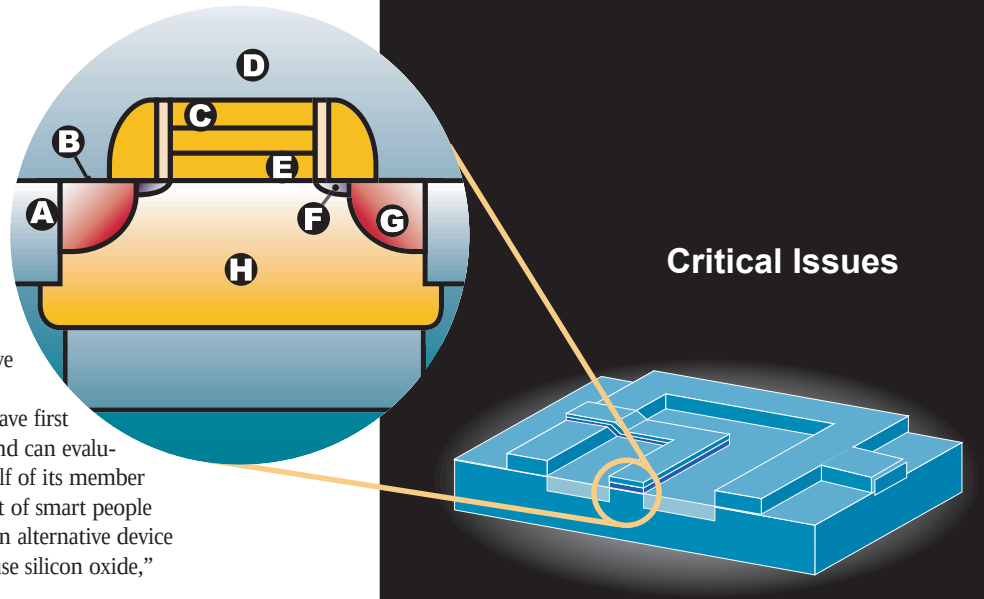
members without divulging company-specific information. The model gives members and suppliers the means to conduct manufacturing cost sensitivity analyses. “This allows our members to understand MOS device challenges and prospective performance at the 100 nm node,” said Peter Zeitzoff, an ISMT fellow who focuses on process integration and NMOS device optimization. “Our member companies can project the main challenges and possible solutions in performance and manufacturing sensitivities for MOS devices at the 100 nm node.”

The modeling analyzes the impact of the physical thickness of the high-k gate dielectric on short channel effects. Moreover, the model helps drive the process control requirements of the ITRS, since input from the International SEMATECH model feeds directly into the ITRS working group deliberations. “By helping our member companies gauge how sensitive the changes will be in the main parameters of device making at the 70 nm node, we set industry direction,” Zeitzoff said.

While International SEMATECH is working toward a high-k material, if that solution is found to be unsuitable to the gate stack challenge, alternatives to high-k materials must be quickly explored and developed. “What if you don't have to use high-k materials, but could use a different structure and still meet Moore's law?” asked Jackson. Because of International SEMATECH's relationships with other research institutes and universities that are exploring alternative ways to meet performance requirements, ISMT will have first access to such structures, and can evaluate their feasibility on behalf of its member companies. “There are a lot of smart people who could come up with an alternative device structure that will let you use silicon oxide,” he said.

"Nevertheless," said Jackson, "International SEMATECH is moving forward rapidly to achieve the right high-k dielectric for future gate stack." To take advantage of gate stack research available worldwide, International SEMATECH this year signed a joint research and development agreement to pursue a new gate stack process for sub-100 nm semiconductor devices with IMEC.

This multi-million dollar international partnership represents a major commitment to accelerate—by as much as two years—efforts to meet the requirements of the ITRS to find a ▶



(**above**)
A depiction of the key front end process challenges as CMOS is scaled. International SEMATECH is focusing its efforts in FEP on high-k materials, ultra shallow junctions, and the total process integration into a CMOS transistor.

Q3
- First high-k transistor build completed • IMEC high-k program initiated
- Acquired AMAT MOCVD tool that gives ISMT capability to deposit high-k materials

Q4
- FEP-RC contract extended from three to five years

FEP (continued)

replacement for current gate stack materials. "This allows International SEMATECH access to outside information, to bring it back into International SEMATECH, and assess its feasibility," said Ed Strickland, a Motorola assignee who serves as program manager for external research and heads the FEP Research Center. The project involving IMEC focuses on advanced gate stack material deposition tasks, electrical/reliability characterization, and replacement transistor gate development for materials characterization, ESH and contamination control. The project will, for the first time, involve placing ISMT assignees outside the U.S.

"We are reaching out to international centers of excellence so that our member companies will achieve their goals," said Jackson. "IMEC provides a crucial piece of the puzzle that will complete the move to new gate stack technology. By leveraging funds through the SRC (Semiconductor Research Corporation) and IMEC, International SEMATECH reduces the risk for its members, and accelerates that knowledge back to our member companies."

ISMT continues to work with the SRC through the FEP Research Center and U.S. universities on fundamental research, and also with equipment suppliers from the U.S., Asia, and Europe. "With our global interactions, we call on the world's resources to help us build a complete set of data on which to help guide the industry to a gate stack replacement," said Jackson. ■

FEP Research Center Moves Closer to High-k Solution

A key link to overcoming the technical challenges necessary for the continued scaling of transistors, the FEP Research Center (FEP-RC) moved forward in two crucial areas during 2000. The first was the narrowing of the choices for high-k dielectrics to three materials. "This enabled researchers to produce actual operating transistors using these new high-k materials and allowed them to begin to characterize these transistors and their operating parameters," said Ed Strickland, program manager of the FEP Research Center, and a Motorola assignee.

The second breakthrough for researchers was the production of very shallow doped junctions using selective epi deposition. "The significance of this discovery is that very shallow junctions can be formed with high concentrations of dopants—higher than possible with current doping processes," said Strickland. High-k and ultra-shallow junctions are two of the three major building blocks to enabling the industry to scale transistors to smaller than 70 nm. "The researchers of the FEP-Research Center are definitely working on the leading edge of these fields. Without these solutions from the Research Center, the industry will not be able to continue to scale transistors smaller and smaller," said Strickland.

"The FEP Research Center has proven to be the best example of cooperative research in the world today," said Martin Giles of Intel and Semiconductor Research Corporation (SRC) Industrial co-chair. "It has already delivered major research results in high-k dielectrics, gate electrodes, and shallow junctions."

A key ingredient to that success has been the excellent collaboration among the different researchers at the various universities. "That synergy among researchers is one of the truly imperative elements of this Research Center," said Strickland.

Established in 1998 in partnership with the SRC, the FEP Research Center is a leader in front end processes research. This cooperative effort, which includes nine U.S. universities, brings together technologists from International SEMATECH and the SRC, their member companies, and equipment suppliers.

"We are attempting to discover solutions for devices beyond 70 nm. We then feed that information back to ISMT. The FEP division then combines that data with process technology to provide an integrated approach to the challenge of scaling below 70 nm," said Strickland.

Set up originally for three years only, the FEP-Research Center was extended for two additional years to 2003. Research into gate electrodes will become a key focus in 2001.

(**above**)
Ed Strickland,
Program Manager,
External Research
and International
SEMATECH/SRC
FEP Research Center

Interconnect: Narrowing the Options, Discovering New Challenges

As copper and low-k dielectrics replace aluminum and silicon dioxide in semiconductor manufacturing, International SEMATECH (ISMT) members look to the Interconnect Division to lead the effort to characterize and screen the many new materials and processes involved in this fundamental shift in interconnect fabrication, so the members can focus on the most promising. Equally important, ISMTs member companies rely on Interconnect working closely with suppliers on the resulting changes required in tools and materials. The Executive Steering Council (ESC) has identified low-k dielectrics as a critical focus area for International SEMATECH, and the Interconnect Division's long-term objective is to study advanced tools, processes, and materials in order to help ISMT members accelerate their use of copper, low-k, and Damascene processing down to 50 nm design rules. The division focuses on both technology development and tool improvement in its efforts to help member companies realize the aggressive interconnect technology roadmap.

The task is not easy. In theory, copper and low-k dielectrics can provide the performance gains the industry will need for the next two to three technology generations. Although copper metalization is moving into mainstream manufacturing, much remains to be done to extend barrier seed and fill technologies, to work with tool suppliers on measurement and reliability issues, and to study future copper scalability. The transition to low-k materials has proven to be far from smooth, given the inherent limitations in the materials themselves and the problematic ways in which these materials interact with manufacturing processes such as patterning, chemical mechanical planarization (CMP), and metalization.

In 2000, the Interconnect Division's major accomplishment was to develop processes and methods that led to the fabrication and electrical test of two-level copper structures in five low-k materials, including two porous materials. These two-level metal tests came after an initial round of physical and electrical evaluations of eight low-k dielectric materials through one-level metal electrical testing. "This is a significant achievement," noted Paul Winebarger, director of the Interconnect Division and a Motorola assignee. "In order to reduce an insulator's dielectric constant, some of the attractive physical properties associated with silicon dioxide will be sacrificed. Our job is to make known the advantages and limitations of these new insulator materials, and to help suppliers and our members develop robust manufacturing solutions to any of their intrinsic material shortcomings. Our work highlighted and gave better understanding to the many engineering tradeoffs that must be considered in the transition to these new advanced interconnect materials."

The various integration approaches evaluated by Interconnect this year were not always good-news stories. International SEMATECH sometimes found new challenges that the industry had not anticipated. Low-k/DUV resist poisoning, for example, was a new problem ISMT characterized extensively and then reported in detail to its members, giving them an informed alert on an unexpected issue.

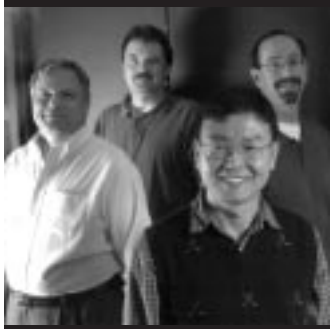
"The fabrication of multi-layer copper interconnects using very low-k materials is proving to be a significant challenge," said Ken Monnig, associate director of Interconnect. "We are learning that it will not be possible to solve these issues by engineering the low-k material alone. Significant engineering will be required in etch, post-etch clean, lithography, CMP, and metalization technology, as well. International SEMATECH has been a pathfinder in bringing these issues to light and providing first-pass solutions to give our members a head-start on their internal product learning curves."

Given this degree of interaction and interdependence among the various technologies, it is not surprising that the activities and programs of the Interconnect Division are highly interrelated.

Copper Metalization

The Copper Metalization program aims to ensure a capable tool and material infrastructure for copper processing. This year's emphasis was on advanced copper barrier and copper seed materials, and their deposition techniques. "Last year we benchmarked the processing capability of most of the PVD [physical vapor deposition], CVD [chemical vapor deposition] and electroplating tools used for barrier, seed, and fill," said Klaus Pfeifer, the Copper Metalization program manager and a Philips assignee. "This year we turned our attention to working with suppliers and universities to identify and characterize advanced CVD copper ►

(**above L-R**)
Ken Monnig, Interconnect Associate Director
Paul Winebarger, Interconnect Director



(**above L-R**)
Bob Havemann, Module Integration Program Manager
Klaus Pfeifer, Copper Metalization Program Manager
Shin Kook Lee, CMP Program Manager
Jeff Wetzel, Low-k Dielectric Program Manager

seed and barrier materials." The copper team conducted electrical via resistance evaluations of four CVD and one ALCVD (atomic layer chemical vapor deposition) copper barrier materials (including TiN, TiSiN, WN, TaN) on dual Damascene structures.

Increasingly thinner copper barriers will be required as feature sizes shrink, and this group continued its work with universities—including The University of Texas at Austin—on the development of advanced next-generation barrier materials, which will ultimately be evaluated for their commercialization potential. The Copper program also continued its efforts to squeeze maximum performance out of copper integrated circuits and foster new solutions for future feature size reductions, by characterizing copper scalability down to 80 nm and looking closely at the effect of line width on copper resistivity.

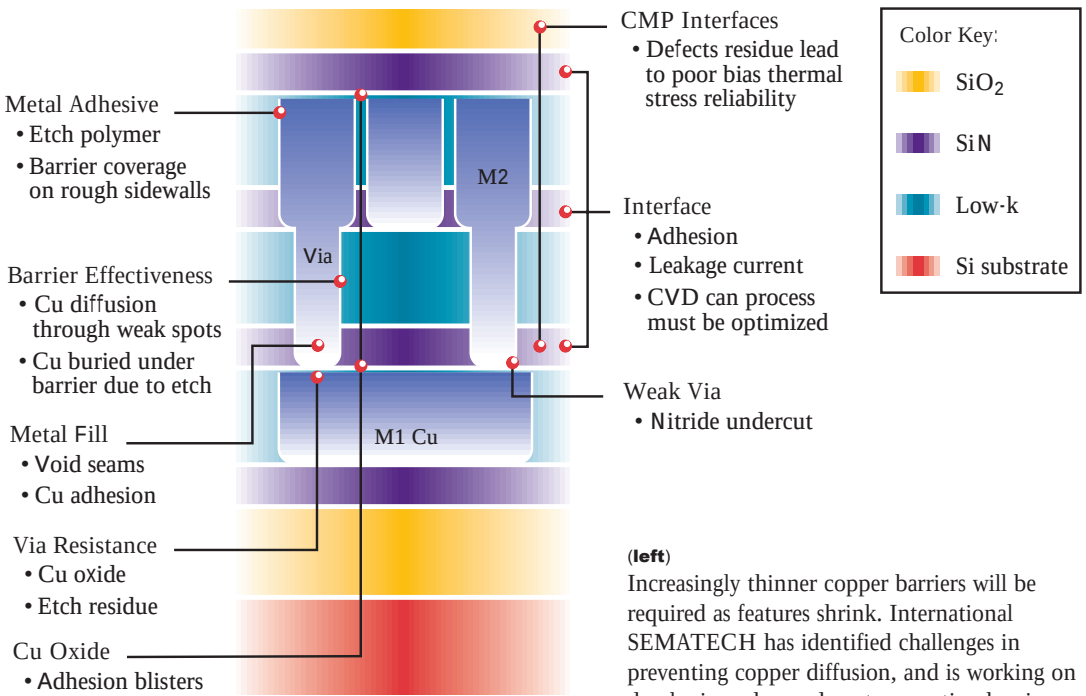
Low-k Dielectrics

Evaluating new low-k dielectric materials and improving supplier capability are the key objectives of ISMT's Low-k Dielectric program. Facing such issues regarding low-k dielectric (<2.5 k) materials as dielectric constant stability, integration-induced damage, resist poisoning, etch/clean damage, adhesion, and CMP damage, the program seeks to develop a mechanistic understanding of these various materials issues and then to feed this information as quickly as possible back to suppliers to drive improvement, and on to the members to help guide their materials decisions.

"Providing the member companies with our physical and electrical characterization data allows them to make more informed decisions about which materials they wish to investigate further," said Jeff Wetzel, Low-k Dielectric program manager on assignment from Motorola. "This gives them early warning on incompatibilities between materials, processes, and the current tool set." In addition to the one-level metal and two-level metal characterizations performed on various low-k materials, with a special emphasis on porous materials, the low-k and CMP groups also established CMP capability on porous low-k films and supported the etch group to complete electrical characterizations of plasma etch/clean and wet cleans on ▶

Preventing Copper Diffusion Creates Challenges

Reliability Concerns Grow as Barrier Thickness Decreases



(**left**)
Increasingly thinner copper barriers will be required as features shrink. International SEMATECH has identified challenges in preventing copper diffusion, and is working on developing advanced next-generation barrier materials that will ultimately be evaluated for their commercialization potential.

timeline

Interconnect Highlights

Q1
- Began one level metal characterization of eight low-k materials

low-k materials. The low-k group continues to benchmark and improve promising low-k dielectric CVD deposition tools.

Module Integration

The Module Integration program expands on the low-k evaluations and quickly identifies the initial problems encountered in building structures in a number of selected immature low-k materials with copper Damascene processing. In 2000, the module integration group performed integration/reliability characterizations of new low-k dielectrics and ultra-thin CVD/ALCVD metal barriers in single and dual copper/Damascene structures. The group fabricated working multi-level metal test vehicles and used those structures to test inter- and intra-level electrical properties, as well as to provide data on high frequency and reliability characteristics of advanced low-k materials. Barrier evaluations included physical characterization (step coverage, adhesion, texture) as well as electrical parametric and reliability testing—for bias thermal stress and electromigration—in integrated dual Damascene structures. According to Bob Havemann, Module Integration program manager and an assignee from Texas Instruments, such efforts serve to detail the interactions of new processes (dual Damascene, plating), materials (copper, barrier, low-k dielectrics) and tools. "This is important information that our members need to support their future technology decisions," stated Havemann.

Chemical Mechanical Planarization

The Chemical Mechanical Planarization (CMP) Program focuses on copper Damascene polish, and works to accelerate CMP consumable development, determine baseline processes, and evaluate unique tools, which may provide more revolutionary approaches to improving CMP capability. In its work this year on CMP/low-k integration and exploring interactions between CMP and new copper barrier materials and copper deposition techniques, the CMP group dealt with issues such as dishing, copper-to-barrier selectivity, selectivity to underlying dielectric, and defectivity.

"As the industry moves to fragile, porous low-k materials, our responsibility is to help create core competency in Damascene polish over porous low-k," said Shin Kook Lee, CMP program manager and senior assignee from Hyundai. "Not only will we work in-house on process development, but we'll also continue our efforts to catalyze suppliers of pads and slurries to address this issue, and we'll work with supplier companies pursuing mainstream polishing solutions and alternatives such as spin etch or electropolish."

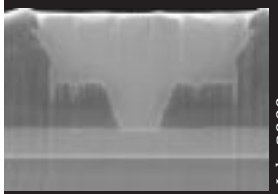
In 2000, the group continued to benchmark and evaluate copper CMP tool suppliers in an effort to accelerate development and identify new equipment approaches that will increase productivity and cost-effectiveness.

Cost is a concern: as circuit designers use more levels of metalization, lowering the cost of CMP becomes more critical.

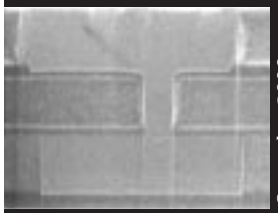
In 2001, Interconnect will focus on three challenges: delivering early evaluations of potential low-k dielectric materials with compatible barrier solutions for the 100/70 nm node; demonstrating candidate low-k barrier solutions with a two-level metal integration process, including baseline reliability; and developing and demonstrating viable Cu/low-k CMP processes for porous low-k materials.

The industry faces a critical challenge in realizing the Roadmap as it considers the next steps in interconnect, after copper and low-k. This so-called "brick wall" looms on the horizon, and in fact, the limits of copper/low-k material capability are not too far away from ISMT's current activities. No known solutions currently exist after the transition to copper and low-k materials. Invention is needed, as is coordination with the design and architecture community that will no doubt contribute to the ultimate solution. ISMT will continue to promote industry coordination in tackling this serious potential show-stopper for discovering new improvements in integrated circuit performance. ■

(**above**)
The Novellus INOVA® is an advanced copper barrier/seed deposition system supporting International SEMATECH's dual Damascene technology.



July 2000



September 2000

(**above**)
Two-level metal dual Damascene results represent the first successful integration of a k=2.2 material.

Q2
- Evaluated performance/reliability of lower-k dielectric barrier(s)

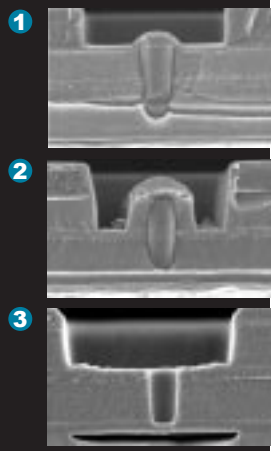
Q3
- Established CMP capability on porous low-k films
- Evaluated electrical via resistance of four CVD and one ALCVD Cu barrier materials on dual Damascene structure
- Completed characterization of Cu scalability down to 80 nm
- High-frequency characterization of low-k materials and interconnect waveguide structures
- Performance, reliability, and packaging assessment of Cu/low-k (k<2.5) material #1

Q4
- Completed integration of four low-k dielectric materials through two level metal
- Final report on 2000 CVD copper fill activity and benchmarking activities
- Completed screening of three seed repair chemistries

patterning

Patterning: Extending 193 nm Technology

(**above**)
Gil Shelden, Patterning Program Manager



1 Via resist poisoning at the subsequent trench photo step (via first approach). Resist poisoning has been observed on a variety of low-k dielectrics.

2 Via poisoning of resist after the trench etch step. A "volcano" surmounts the via.

3 A dual top hard mask approach has been used instead of the via first approach to eliminate the resist poisoning problem.

October 1, 2000 marked the operational debut of the Patterning program, drawing together in one cross-functional program activities which had been spread across Interconnect, Lithography, and the Advanced Technology Development Facility (ATDF). Now the champion for International SEMATECH's (ISMT's) 193 nm Extension key focus area, the Patterning program's overall objective is to ensure that the 193 nm/157 nm technology is ready on time, and is a viable and cost-effective answer to next-generation feature requirements.

"193 nm patterning is now the majority choice for the 90 nm node (2004)," said Gil Shelden, Patterning program manager. "And it will likely be pushed farther as the ITRS accelerates. The new Patterning program offers unified direction in our effort to stay on the 193 nm productivity curve as long as possible."

Optical Extension

ISMT's Optical Extension program emphasized three 193 nm process development and enhancement techniques:

- Resist Performance—Currently available resist materials need more characterization and performance improvements in etch resistance and selectivity; edge roughness, material stability, substrate compatibility, cost, and material availability remain manufacturing concerns. During the year, ISMT benchmarked 18 different 193 nm resists. Although excellent progress is being made, none of the currently available materials is suitable for 100 nm node production requirements.
- Degradation of Optical Material—193 nm ArF Excimer wavelength technology requires development of special optical materials, since the higher energy of 193 nm illumination creates greater potential for material degradation. In 2000, ISMT completed accelerated life testing of 193 nm materials including pellicles and fused silica for mask blanks. Several promising materials have been identified, but concerns remain about induced birefringence.
- Phase Shift Masks (PSMs)—Preliminary testing of alternating and attenuated PSMs has made it clear that the technology still needs development, especially in the area of attenuated phase shift materials for contacts, vias and trenches. Alternating PSM technology, used extensively to improve isolated line (gate) critical dimension (CD) control, has limited benefits for dense lines and spaces.

Etch

The Etch group performed etch characterization of four low-k materials, investigated the root causes for the low-k/DUV resist poisoning phenomenon, and completed electrical characterizations of the impact of several plasma etch/clean and wet clean processes on low-k materials. Moreover, working closely with the Front End Processes (FEP) Division on how to etch the next generation of gate stack materials, the Etch group achieved initial 193 nm gate etch results for both SiO_2 and ZrO_2 gates. Going forward, the Etch Tools program will support key Interconnect, FEP, and Lithography initiatives by providing etch/cleans process and tool evaluations in three areas: low-k materials, advanced gate stack materials, and 193 nm resist patterning interactions. In 2000, the majority of this work was executed at 248 nm; in 2001, it is anticipated the work will extend to 193 nm. In addition to the challenges of smaller feature size and reduced depth of field, a new set of materials interaction challenges will emerge when dealing with new resist systems.

The Etch Chemistry and Diagnostics program focused its efforts on collecting diagnostic data for C_xF_x species and on extensive modeling of oxide etch rates in C_2F_6. Next year this program will produce basic plasma chemistry database sets to support individual member company development of plasma modeling codes.

ATDF/Tool Support

Involved with the development of 193 nm technology since the early 1990s, ISMT received its first 193 nm limited field 0.6 NA microstepper in 1996 to support resist development. ISMT later partnered with DNS and obtained a state-of-the-art track system to interface with an SVGL MS193 full-field 0.6 NA 193 nm scanner. While dense contacts/vias continue to be the biggest challenge, standard binary reticles are currently producing 130 nm dense features with reasonable process latitude and depth of focus (0.6 µm); ISMT is achieving 100 nm gates with binary plates, and 70 nm gates with phase shift technology. ■

timeline

Patterning Highlights

Q2
- 0.6NA 193nm SVGL tool installed and printing
- Obtained diagnostic data collection for C_xF_x species

Q3
- Delivered 3D EMF software; electrical characterization of several low-k clean processes

Q4
- 193 nm gate etch results obtained • completed etch characterization of four low-k materials • Low-k resist poisoning characterization initiated and analyzed

Metrology/Yield Management Tools: Accelerating Innovative Solutions

During 2000, International SEMATECH (ISMT) launched a major effort to reduce the limitations facing future metrology and yield management technology by consolidating Lithography Metrology, FEOL/BEOL Metrology, and Yield Management Tools into a new, more focused Metrology/Yield Management Tools (M/YMT) Program. The program's critical objective is to ensure the availability of metrology and yield management tools for the 100 nm node and beyond, by accelerating the availability of metrology in CD (critical dimension), overlay, gate stack (high-k), ultra shallow junction, and low-k, and by accelerating yield management solutions in defect detection, yield modeling, and defect sourcing.

"New lithography capabilities for reduced feature sizes, plus the introduction of new materials such as low-k and high-k dielectrics, are pushing metrology toward innovative solutions," stated Alain Diebold, M/YMT technical manager. "For the industry to stay on the Roadmap, new methods of characterizing masks, measuring process variation, and ensuring product quality must be found." Ron Remke, program manager and a Lucent/Agere assignee, added, "As geometries shrink, we increase the detrimental impacts of defects, making defect detection, measurement, and characterization more important than ever."

Highlighting the year's efforts in M/YMT were significant improvements in the design, effectiveness, and precision of next-generation metrology tools, particularly in their ability to interface with new processes and materials. M/YMT also spearheaded a set of yield management tool benchmarking, inspection and software projects designed to improve member companies' yields as rapidly as possible. Key achievements include:

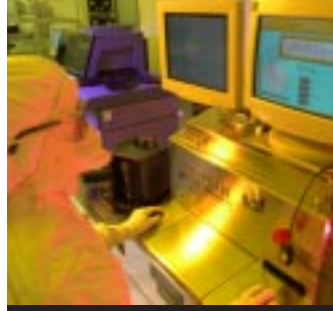
- Optical models for measuring oxynitride and high-k materials for advanced gate stacks
- Specifications for a next-generation CD scanning electron microscope (SEM), developed in conjunction with four major suppliers
- Testing software designed to improve the resolution, precision, and 3-D capabilities of CD-SEMs, in cooperation with the National Institute of Standards and Technology (NIST)
- Testing reference wafers for a promising in-line junction depth measurement tool
- Benchmarking the defect inspection tools of six key suppliers, and developing a new reticle set to aid in evaluating defect inspection equipment
- Investigating the defectivity of low-k dielectric films and the ability of existing tools to inspect for defects on low-k films
- Evaluating new software tools to identify particle-sensitive circuit areas
- Evaluating commercial software for defect mapping and image retrieval

Metrology/Yield Management Tools Initiative

This new model of collaboration between ISMT and leading industry suppliers such as Therma-Wave, Boxer-Cross, Hitachi, KLA-Tencor, Philips Analytical, and Veeco, launched during the summer, will help the industry surmount the critical metrology and yield management challenges posed by the *International Technology Roadmap for Semiconductors* (ITRS) by accelerating next generation processing through testing of new tools. "The Initiative provides suppliers with access to new technology generations and new materials," said Diebold. "Tools for in-line ellipsometry, in-line non-contact capacitance-voltage, in-line junction depth measurement, CD measurement, defect detection, and in-line measurement of seed copper/barrier thickness and CMP control are all involved in this groundbreaking cooperative effort to evaluate equipment at the 130 nm and 100 nm nodes, and to develop metrology and yield management capabilities for critical areas such as gate stack, low-k, and 193 nm optical extension."

Yield Council

ISMT's Yield Council is a long-standing member company forum that meets three times a year to share best practices in rapid yield learning and to benchmark yield improvement activities. "The most important thing you can improve in manufacturing is your yield, because that determines your profit margin and increases your capacity," stated Remke. "Over the many years of the Yield Council's existence, it has consistently rated near the top for member company value. Member companies report to us that the information and benchmarking results that they receive as part of the Yield Council are not available from any other source." ■



(**above**)
Therma-Wave Opti-Probe 5240D with scatterometry capability

(**above**)
Ron Remke, M/YMT Program Manager

(**above**)
Alain Diebold, M/YMT Technical Manager

timeline
Metrology/YMT Highlights

Q1
- Therma-Wave Opti-Probe operational
- Completed Critical Area Extraction (CAE) software assessment

Q2
- Extended CD-SEM to 3D NIST software given to member companies

Q3
- Initial high-k optical metrology for ZrO_2/HfO_2 in ATDF
- Benchmarked four leading defect detection equipment suppliers using induced defect wafers
- Commercialization contract signed for Computer Aided Fault to Defect Mapping (CAFDM) software
- Launched Metrology/Yield Management Tools Initiative
- Precision of thin gate metrology improved using desorber on Therma-Wave Opti-Probe

Q4
- NIST test of SRC Nanotip source for extending CD-SEM to future generations
- Beyond CD-SEM—SRC electron holography proof of concept interim report
- 130 nm/100 nm overlay tool capability specification
- Quantox delivered

esh
Environment, Safety and Health: Protecting the Environment, Saving Resources

(**above**) Coleen Miller, ESH Director

(**above L-R**) Walter Worth, Environmental Protection Program Manager, Peter Dahlgren, Worker Protection Program Manager

Dedicated to helping the industry take the lead and realize the Roadmap in environmental, safety, and health (ESH) issues, International SEMATECH's (ISMT's) ESH Division in 2000 demonstrated the feasibility of a more benign chemical process for resist stripping, spearheaded a 40 percent reduction in ultrapure water (UPW) consumption among member company fabs, and helped a member company rein-in energy costs for manufacturing. Along with advances in new technologies for reduced PFC emissions and improved management practices for leading-edge chemicals, these improvements are enabling the industry to realize the *International Technology Roadmap for Semiconductors* (ITRS) goal of fabs with lower costs and fewer environmental issues.

Ozonated Deionized (DI) Water Can Replace Sulfuric Acid in Resist-Stripping

During the year, member company and supplier engineers successfully demonstrated and benchmarked the use of ozonated DI water (DI/O_3) in resist stripping processes as a substitute for SPM, a mixture of sulfuric acid and hydrogen peroxide. The new method, engineers found, is comparable in performance and cost with SPM, and could replace it in many applications.

Environment, Safety and Health Director Coleen Miller, a Texas Instruments assignee, pointed out that reduction of chemicals used in the industry is one of the key ITRS ESH elements. "There's a general trend toward reducing chemicals in favor of benign chemistries, so that the manufacturing process is environmentally friendly and safer across the board," Miller said. "The idea is to encourage the use of these chemistries without compromising production—such as yield, throughput and process performance—or financial goals."

Member Fabs Cut Ultrapure Water (UPW) Consumption by 40 percent

A survey taken by ISMT showed that between 1996 and 1999 the UPW use within member company fabs was reduced by as much as 40 percent. Recommendations from International SEMATECH studies over that same time period involved optimizing rinse tank design; eliminating over-rinsing; improving idle flow rate; replacing overflow rinses with quick-dump and spray rinses; and practicing UPW recycling and reuse.

The 1999 survey also showed that the average amount of UPW used in production per square centimeter of silicon (L/cm^2) dropped from 16.9 to 9.5 L/cm^2 after study recommendations were implemented. The most optimized fab operated at a UPW flow of 7.2 L/cm^2. This amounts to significant progress toward the ITRS goal of 6-8 L/cm^2 of silicon by 2001 in a state-of-the-art fab.

Miller noted that the increasing complexity of high-performance circuit manufacturing has brought an accompanying demand for new chemicals and greater volumes of UPW. The cost of large-scale UPW plants and treatment/disposal facilities are beginning to add significantly to overall cost of ownership.

"One solution is to reduce the overall use of water, thereby lowering fixed and operating costs and putting less strain on the local environment," Miller said. "This benchmarking project has allowed us to put together all the options for a company to pursue as it chooses."

Members Show Significant Reductions in Exhaust Rates, HEPA Velocities

During 2000, ESH projects focused on equipment exhaust optimization and HEPA velocity reduction demonstrations at member company fabs have provided member companies with immediate savings in equipment and facility energy consumption.

According to Miller, exhaust optimization projects are demonstrating an average potential for 50 percent reductions in exhaust requirements while still meeting SEMI and member company safety requirements. Sometimes the savings are even greater: in one study, engineers found that the design specification for an etch tool (in cubic feet per minute) was nearly seven times the amount actually needed to meet safety requirements.

Meanwhile, the ESH Division's demonstrations in HEPA velocity reduction have shown that members can reduce air handler energy consumption by 20-30 percent and still maintain cleanroom specifications. In one instance, a member company estimates it will save $100,000 annually in energy costs by ▶

timeline
ESH Highlights

Q1
- HEPA velocity reduction at AMD

Q2
- HEPA velocity optimization at HP
- Tool exhaust reduction study at HP

Q3
- Evaluation of catalytic abatement for PFCs
- Prioritization of ESH data types

Q4
- DI/ozone resist strip demo in spray processor
- Benchmarking of water use in CMP tools
- Beta test of remote plasma for DxL chamber cleans
- Comparison of SEMI S2 and CE Marking
- White paper on novel wafer cleans
- Tool energy analysis at AMD

reducing fan speeds by 30 percent in one of its fabs.

"HEPA velocity reductions represent a potential for a huge cut from an energy perspective," said Miller. "You can get an environmental benefit that also provides a benefit to the business—a definite win-win situation."

The ITRS specifies that energy consumption by process equipment and facilities infrastructure should fall within a range of 0.5-0.7 kilowatts per hour per square centimeter of silicon (kWh/sq cm^2). The division's tool and fab energy reduction projects will remain focused on demonstrating energy reduction techniques to reduce members' energy consumption. This will enable members and suppliers to work together to meet the goal of more efficient factory and equipment designs.

Two New Technologies Demonstrated for Reducing PFC Emissions

In keeping with international and member company goals to reduce emissions of perfluorocompounds (PFCs) used in semiconductor manufacturing, ESH-led projects successfully demonstrated the effectiveness of two new technologies to treat the chemicals that contribute to global warming.

The first demonstration showed the applicability of remote cleaning to a chemical vapor deposition tool abundant in the industry. This technology replaces C_2F_6 with NF_3. In the most recent study, engineers found that using this technology had no adverse effects on deposited film parameters or the reactor's quartz window—and resulted in a remarkable 65 percent reduction in clean time, thus allowing greater tool throughput.

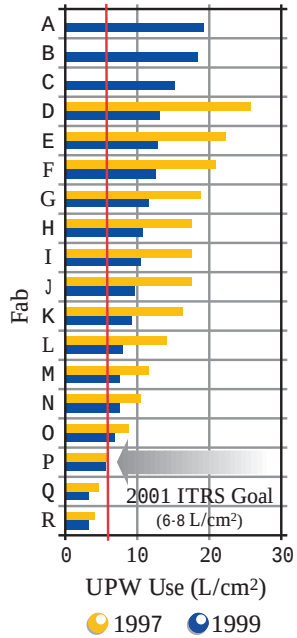
The second advance was the successful demonstration of a catalytic PFC abatement technology on a manufacturing tool. One member company tested a super catalytic decomposition system, consisting of two integral water scrubbers and a heated catalyst bed that breaks down stable PFC gases to HF, SO_2, and CO_2. Tests over a ten-month period showed that more than 99 percent of the gases were destroyed without loss of catalyst efficiency.

"These technologies provide two more options for reducing PFC emissions from semiconductor equipment," said Walter Worth, Environmental Protection program manager. "They are important because the industry must have as many technology options as possible to provide a flexible PFC emission reduction strategy to accommodate the differences between old versus new fabs, and small versus large fabs."

Matrix Developed for Obtaining ESH Data on New Chemicals

The ITRS has identified management of chemicals and materials as one of the five difficult ESH challenges. International SEMATECH is working with member companies, suppliers, and other research partners to accelerate the availability of ESH information for new chemicals. "International SEMATECH's project is about getting direction from our members about what information we need, and when we need it" said Peter Dahlgren, Worker Protection program manager and an assignee from IBM. "We are working closely with suppliers to help define and obtain early information on chemicals. Our members will use this data in making new process technology and associated ESH control decisions." ■

Water Use in Semiconductor Plants



(**above**) An International SEMATECH survey showed that the average amount of Ultrapure Water used in production per square centimeter of silicon (L/cm^2) dropped from 16.9 to 9.5 L/cm^2 after study recommendations were implemented.

ITRS & Focus Area Mapping for ESH *(5 Year Strategy)*

ITRS ESH Challenges	Post 193 nm	193 nm Extension	Mask Cost and Availability	Low-k Materials	Gate Stack USJ	Manufacturing Effectiveness
Chemicals, Materials and Equipment Management	ESH Chemical Data Strategy, Radiation By-Products	ESH Chemical Data Strategy	ESH Chemical Data Strategy	ESH Chemical Data Strategy, Novel Wafer Cleaning	ESH Chemical Data Strategy, Novel Wafer Cleaning	ESH Chemical Data Strategy
Climate Change Mitigation			Low GWP Chemicals	Energy Use Reduction and Low GWP Chemicals	Energy Use Reduction and Low GWP Chemicals	Energy Use Reduction
Workplace Protection	Coordinate and Apply ESH Standards	Coordinate and Apply ESH Standards	Coordinate and Apply ESH Standards	Coordinate and Apply ESH Standards	Coordinate and Apply ESH Standards	Coordinate Equip. Safety Standards
Resource Conservation	Alternative Patterning Methods	Reduced Chemical Usage	Alternative Chemicals and Materials	Alternate Cleans and Efficient CMP	Alternate Cleans	Maximize Efficiency
ESH Design and Measurement Methods	Quantify ESH Impact			Quantify ESH Impact	Quantify ESH Impact	Quantify ESH Impact

mm&p

Manufacturing Methods & Productivity: Setting the Standard for Industry Effectiveness

(**above L-R**)
Randy Goodall, Manufacturing Methods & Productivity Associate Director
Ken Vandehey, EPITs Program Manager
Scott Kramer, MM&P Director
Harvey Wohlwend, e-Diagnostics Program Manager

Transforming knowledge gained from existing factories into productivity improvements for the future is key to International SEMATECH's (ISMT's) manufacturing effectiveness strategy.

ISMT's Manufacturing Methods and Productivity (MM&P) Division provides members with an ongoing competitive advantage in their production operations and manufacturing effectiveness through programs that involve installed base equipment and fabs, as well as future fabs.

"The unique aspect of many of our programs is the exchange of information that takes place between the member companies—companies that outside of International SEMATECH are competitors," said Scott Kramer, director of MM&P. "But the result is leading-edge fab technology that keeps all our members ahead of the curve."

The Manufacturing Methods Council, a group of member company fab and operations managers who meet regularly, continued this year to share their expertise with one another. Through extensive, anonymous benchmarking, sharing of best-known methods, and workshops on common problems, the Council targets areas for improvement in IC manufacturing and generates critical data for validating models used to study improvement strategies. Topics explored in 2000 range from reduction of test wafers to better glove and gowning procedures.

e-Diagnostics Guidelines

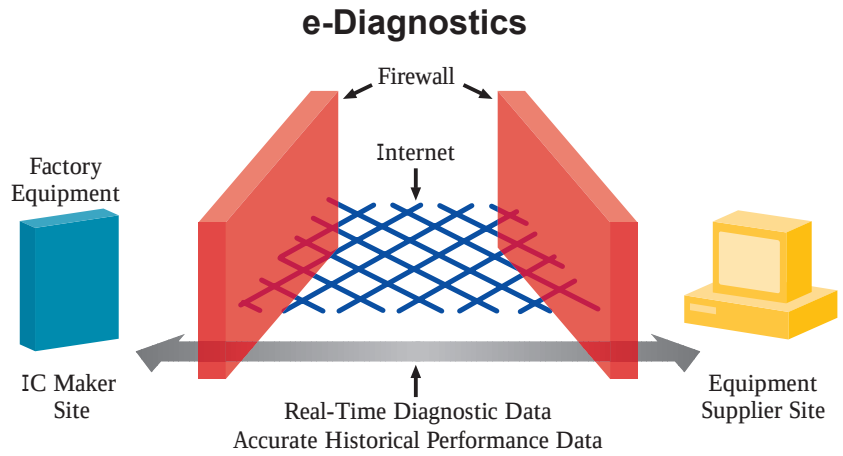
In April, International SEMATECH's Board of Directors called for the creation at "Internet speed" of an accelerated e-Diagnostics program to drive pre-competitive technology and standards development within the industry. A working group under the leadership of Harvey Wohlwend, e-Diagnostics program manager, delivered the first set of supplier requirements within two months. "It is imperative that we have open standards to make sure that the entire semiconductor and equipment industry can take advantage of the Internet. As a result of our program, we hope to see revolutionary improvements in equipment up-time among our member companies," said Wohlwend.

Previously, semiconductor fabs had not broadly incorporated e-Diagnostics solutions out of concern for security issues, lack of standards, and the existence of diverse supplier support. "Our e-Diagnostics program teams are actively working on security and standards," said Wohlwend. "Because of the support and active engagement of suppliers, we foresee a smooth transition to standardized, industry-wide e-Diagnostics."

Added Michael Splinter, executive vice president and general manager of Intel's Technology and Manufacturing Group and ISMT board member, "International SEMATECH's e-Diagnostic program is key to higher productivity of our equipment and processes."

300 mm FOUP-to-Loadport Interoperability Guidelines

Standard front-opening unified pods (FOUPs) and loadports are the building blocks for automating the movement of wafers in and out of process equipment in 300 mm factories. Teams from both the Automated Material Handling (AMH) program and the Standards program drove industry-wide consensus on 300 mm FOUP-to-Loadport Interoperability Guidelines and Measurement Methods. As a result, ISMT has made available a unified checklist for suppliers to test the interface of loadports and 300 mm FOUPs to insure compatibility. The interoperability of 300 mm wafer carriers (FOUPS) to process equipment loadports has high impact on installation and operation of 300 mm factories. Published through SEMI, these guidelines were developed in collaboration with Selete, a Japanese consortium of IC makers, and the Fraunhofer Institute. ▶



(**left**)
Remote diagnostics capability will give member companies and suppliers vast improvements in tool up-time.

MM&P (continued)

"A typical factory will have over 500 loadports and several thousand FOUPs," said Marlin Shopbell, Automated Material Handling (AMH) program manager and AMD assignee. "Unless the reliability of FOUP-to-loadport operation approaches 100 percent, interoperability failures will be a daily restraint to manufacturing."

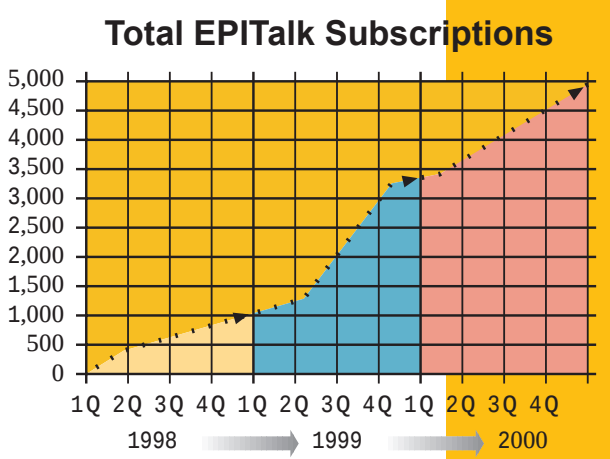
The AMH and Standards teams collaborated with Selete in identifying the key points of measurement needed to ensure the compatibility of loadports and FOUPs, and in the evaluation of jigs and fixtures to measure compliance to the standards.

300 mm Equipment Software Functionality Requirements

One of the key requirements for 300 mm factories is full or total automation. The Standards and Guidelines program achieved consensus with Selete on software requirements for 300 mm production equipment. The result: publication of the 300 mm Equipment Integration and Automation Software Functionality Requirements, which provide a set of base equipment functional requirements and sample base equipment operational scenarios. This consensus provides guidance to suppliers on the interpretation and application of the SEMI standards and reduces the variations across equipment. Three workshops held last year helped to educate equipment suppliers and accelerate software implementations to meet member company production schedules. "Suppliers have IC manufacturer guidance on what they need to implement globally as a standard set of functionalities," said Jackie Ferrell, ISMT Standards and Guidelines program manager. "The more consensus we can achieve, and the more unified guidance we provide to suppliers, the less suppliers have to customize. This translates into faster installation and ramp-up, increased software functionality and reliability, and higher factory productivity."

Industry Economic Model

To help suppliers and member companies stay on the current fast-paced productivity curve, the Productivity Analysis program developed in 2000 an Industry Economic Model on the dynamics of the chip-making business, including the equipment and materials supply chain. This tool will help ISMT's member companies and suppliers explore various technology assumptions and business scenarios so they can prepare for downturns, anticipate upturns, and adjust capacity accordingly. "This gives suppliers and our members a platform from which to carry on a dialogue about technological changes ▶



(**above**)
In 2000, EPITalk logged more than 2,100 messages from member companies and suppliers.

EPITalk Delivers 24/7 Response at Internet Speed

Gareth Bignell, Ion Implantation section manager at STMicroelectronics in Crolles, France, had some questions about converting the implant area from high-pressure Arsine, Phosphine and compressed bottles to safe delivery system (SDS) bottles, a major undertaking that, nevertheless, results in higher fab productivity and wafer throughput. He turned to EPITalk, International SEMATECH's server-based e-mail distribution network that allows participants to communicate real-time equipment issues and share multiple solutions, sometimes within a matter of hours. Bignell got his answer within 24 hours.

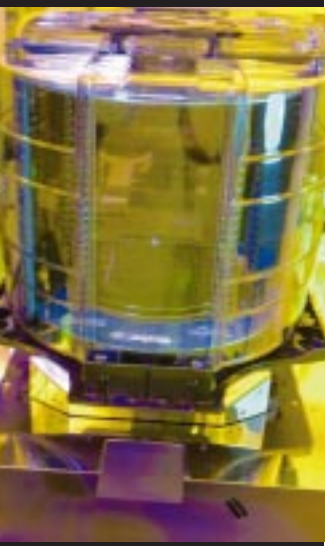
Because the gas in an SDS bottle is not pressurized, but instead trapped inside a proprietary form of Carbon, accidentally opening the bottle or breaking a gas line presents virtually no health risks. The same error on a pressurized HP bottle, however, can create the dangerous release of gas in fewer than two seconds.

In addition, SDS bottles are longer lasting than the HP bottles, requiring less frequent change-outs. Bottle change-outs can require evacuation of the implanter building, a 45 minute-operation that takes 10 workers off of the production line. "I wanted to know what other fabs do when changing bottles. I was hoping that some fabs would have gone to a no-evacuation procedure," said Bignell.

So he sent an EPITalk e-mail at 3:36 p.m. on a Monday asking member companies for their experiences with the SDS gas bottle change procedures. Six minutes later, Philips responded with an outline of its procedures at its Albuquerque, New Mexico fab. AMD, Intel, Infineon, IBM, Lucent and VLSI followed suit, and by 1:15 p.m. the next day, International SEMATECH had forwarded all of these responses to Bignell.

"The speed of the response was excellent," he said. "The value of the EPITalk was to add pieces to the overall jigsaw puzzle. These pieces, along with our own ideas and the help offered by the SDS gas supplier, enabled us to establish a coherent 100 percent SDS conversion plan, which respects our strict ESH culture and our commercial objectives," said Bignell. "Perhaps the most useful information was the reference to SDS pressure increasing with temperature, and the advice to store the bottle in a controlled environment 12 or 24 hours before use."

EPITalk, established in 1998, provides member companies with technical information within hours of the posting of a question. In 2000, EPITalk registered more than 2,100 messages from member companies and tool suppliers seeking answers to questions ranging from meeting dates to chamber cleaning procedures.



(**above & below**) Standard front-opening unified pods (FOUPs), shown here, are the building blocks for automating the movement of wafers in and out of process equipment in 300 mm factories.

MM&P (continued)

and their impact on the costs of realizing the Roadmap," said Randy Goodall, associate director of MM&P. While not a forecasting tool, the model provides unbiased sensitivity analysis as a foundation for building common understanding between equipment suppliers and IC manufacturers. "We are providing a tool for executives that lets them anticipate and discuss various economic scenarios," said Denis Fandel, project manager and IBM assignee.

EPITs Beta Sites

MM&P's Equipment Productivity Improvement Teams (EPITs) focus on installed base equipment improvements and cost of ownership reductions by partnering with equipment suppliers in continuous improvement projects. Through the EPITs Beta Site program, member company and supplier engineers collaborate in identifying productivity obstacles, testing solutions, and sharing results. During 2000, EPITs participants engaged in over 75 beta test site activities at all thirteen of the member companies.

"The beta site activity provides an advantage to both member companies and suppliers," said Ken Vandehey, EPITs program manager and HP assignee. "Member companies benefit by receiving and evaluating pre-release tool enhancements that will ultimately reduce the cost of ownership for their installed base. Suppliers benefit by receiving early access to the evaluation results—directly from their customers—and can act accordingly to incorporate this information into future equipment."

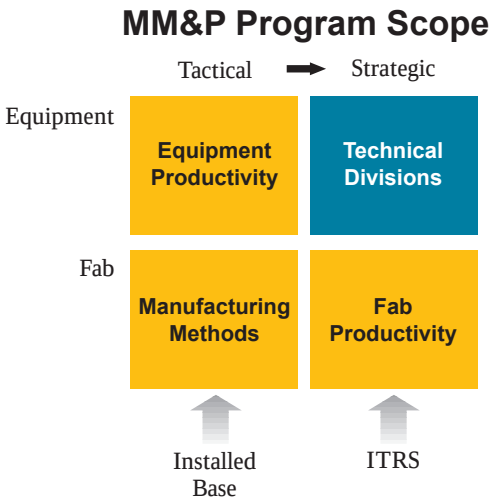
In 2000, ISMT implemented the first semi-annual Beta Site Awards to recognize member company efforts in the categories of Most Innovative Beta Site, Best Beta Site Report, and Beta Site Yielding the Best ROI.

The award for Most Innovative Beta Site for the first half of 2000 involved a fiber optic camera used on the Applied Materials Endura system to help improve the calibration of the robot to the process chambers. Previously, the only means of performing the calibration of this robot was to open the chamber and look inside, which required a time-consuming post-calibration chamber clean. The fiber optic camera system allows the calibration to take place under vacuum conditions. Eliminating the need to manually enter the system will increase availability and reduce consumable costs as a result of the extended time between chamber cleans and kit changes. Installed at three sites, the camera system will yield results by 1Q of 2001 and will be available to all member companies.

The award for the Best Beta Site Report for the first half of 2000 resulted from evaluation of a new etch chamber. One member company, in the process of evaluating a new etch chamber at a cost of several hundred thousand dollars, sought support to perform the evaluation. In return, the other twelve member companies received the complete results. "This evaluation will certainly benefit those who are interested in the chamber's performance capabilities," said Vandehey. "Member companies now have access to this information without the associated chamber cost and engineering expenses."

The award for Beta Site Yielding the Best ROI in the first half of 2000 stemmed from reductions in preventable maintenance time which was significantly reduced after evaluating a Ferrofluidic seal for the Novellus C-1 Dielectric CVD system. As a result of the project, the scheduled maintenance was reduced from 252 hours-per-year using the previous style T-seal, to only 72 hours-per-year. The annual cost savings associated with the reduced maintenance and increased wafer capacity is in the hundreds of thousands of dollars for a fab with an average of five such tools.

"You have the top chipmakers in the world getting together and comparing equipment performance results," said Vandehey. "Only the members of this consortium get that. There's no consultant who can provide this type of information." ■



(**above**) MM&P comprises three major program areas. Equipment Productivity delivers tactical value by focusing on installed-base equipment. Manufacturing Methods also returns tactical value by identifying productivity improvements for existing fabs. In contrast, Fab Productivity develops strategic value through projects that are driven by the ITRS.

ATDF: Improving Cycle Times

Cycle time—a key indicator of productivity—decreased in the ATDF (Advanced Technology Development Facility) in 2000 through streamlining, communicating and consolidating. By reducing cycle time in the ATDF, International SEMATECH (ISMT) has added to the number of research learning cycles that can be provided to technical division projects. "This accelerates the amount of research we can do and helps our technical divisions by completing projects ahead of time," said Robert Swartwout, manager of manufacturing operations.

The 50-67 percent decrease in cycle time resulted from streamlining the workflow in the ATDF, said Juergen Woehl, an Infineon assignee who was named director of the ATDF in May. "We eliminated waste and put our resources where they would be used most efficiently. We believe that our ATDF is the best research fab anywhere."

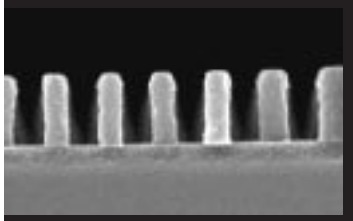
Among the changes that contributed to the improvement in cycle time was identifying ownership of tools in the fab. In the past, a technical division was responsible for a tool if that tool performed the majority of its work for that technical area. "But," said Woehl, "This practice kept the fab from performing at its peak capability. To improve, we put a stake in the ground and said that all tools, no matter who paid for them, are owned by the ATDF." Consequently, the ATDF schedules the tools and coordinates project lots, moving them more rapidly through the line. "The key issue was not a lack of performance," said Woehl. "It was more about communication and how we work."

ISMT instituted several other programs that led to the decrease in cycle time and will contribute to the continued improvements in the ATDF operations. "These steps will help us make a target of three moves per day by June of 2001, and will make us a world-class facility in R&D because decreased cycle time goes hand in hand with improved quality," said Woehl.

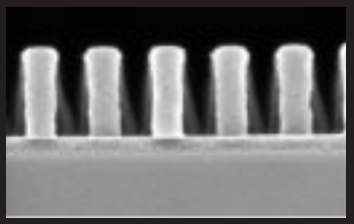
The additional steps include:

- Just-in-time line loading. "We put specially-trained technicians on the second and third shifts to analyze the line and start material into the line based on real-time conditions," said Swartwout. "Historically, it was inevitable that when a tool went down or the conditions in the line changed, the material would sit in front of a down tool while the cycle time clock was running. With just-in-time load ing," he said, "we are pushing material into the line across the 24 hour time clock, and that has helped us to drive more material through the line at a faster rate."

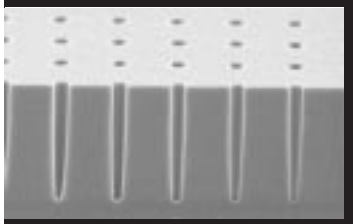
- Expanded Operating Hours. Further improvements are planned in January 2001 when the ATDF goes from a five-day to a seven-day-per-week operation. "We will be operating 24/7: 24 hours a day, seven days a week," said Swartwout. "This new schedule will drive down cycle times further because it lets us keep material moving across the weekend." As a result, there is essentially no ramp time for the tools in ISMT's ATDF. "This has a positive impact on the tools themselves," ▶



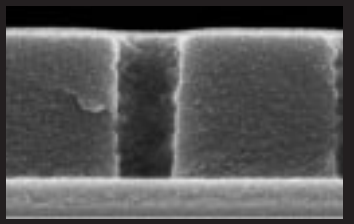
(above)
100 nm dense lines with alternated phase shift mask at 0.4 µm depth of focus



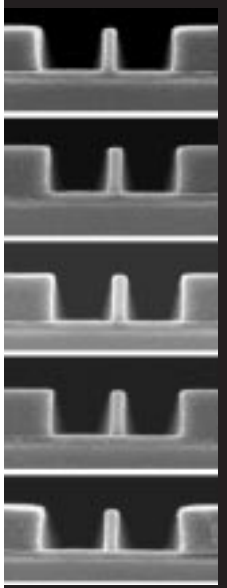
(above)
130 nm dense lines with a binary reticle at 0.8 µm depth of focus



(above)
130 nm contacts etched in oxide (no hard mask) with a 7.7 to 1 aspect ratio



(above)
140 nm contact with a 6% attenuated phase shift mask at 0.7 µm depth of focus



(left)
65 nm isolated lines with phase shift mask at various depths of focus

ATDF (continued)

(**above L-R**) Dan Holladay, Associate ATDF Director, Bob Swartwout, Manager of Manufacturing Operations, Juergen Woehl, ATDF Director

said Swartwout. "We gain time by eliminating the need to requalify those tools," he said.

- Reiterating ISMT's priorities. Expanding the ATDF hours will allow ISMT to increase the number of projects that can be performed, although member company projects will continue to get priority over all other projects. "We are here first and foremost to perform the internal projects that our member companies want done," said Woehl.

- Reduction of ITPs (Interrupts to Production) caused by unanticipated or weather-related power outages. By benchmarking member company fabs, it became apparent that the 50 ITPs in the ATDF were "unacceptable" Woehl said. The goal for 2001 is now 24 ITPs, which will be accomplished through upgrades and facilities improvements.

Other key accomplishments in the ATDF during 2000:

- ISMT gained the ability to provide advanced 193 nm resist patterns to the ISMT technical divisions in 2000 with the installation and qualification of a full-field 193 nm scanner from Silicon Valley Group (SVG) and a Dainippon Screen (DNS) SK-2000 state-of-the-art track. The DNS system was one of the first installed in the U.S., and gives ISMT resist processing capability to perform sub-130 nm lithography. This equipment provides early learning on 193 nm lithography and drives the 193 optical extension program, one of ISMT's six key focus areas. The Micrascan 193 nm ArF Exposure system gives ISMT its first full-field 193 nm scanner to conduct resist and reticle development work at and below 130 nm feature sizes. It also provides the ATDF with the lithography capability to support advanced work in Interconnect and Front End Processes by providing leading-edge resist features. With the development of 193 nm optical extension techniques and resist processing improvements, the ATDF plans to extend this tool set to the 100 nm node. The SVG scanner will also be the primary lithography tool used in the new ISMT Patterning initiative.

- The ATDF will accept delivery of a next-generation High NA (0.75) 193 nm scanner in 1Q 2003, which will be used to develop optical patterning capabilities at and below the 100 nm node. One of the first 157 nm full-field systems has been secured for the ATDF and is scheduled to arrive in 4Q 2002. This advanced pre-production 157 nm scanner will support the process maturity of 157 nm technology.

- ISMT's 300 mm program was transferred into the ATDF in 1999, and provided 7,000 300 mm test wafers to member companies in 2000. By supplying patterned 300 mm wafers for member companies starting up their 300 mm pilot lines, ISMT helped accelerate the critical time window between tool acceptance and wafer starts. The ATDF has also accelerated the development of the 300 mm technology by providing wafers to tool suppliers for 300 mm equipment development and process characterization.

The ATDF also added numerous new process capabilities that support ISMT's technical divisions and help keep on or ahead of the International Technology Roadmap for Semiconductors (ITRS):

- The ability to perform state-of-the-art advanced pre-gate clean treatment on devices built with high-k materials that are critical to gate stack.

- Implementation of a shallow trench isolation (STI) process. The ATDF now has isolation capability commensurate with the technology nodes in which it is working. The improved planarity achieved by STI enables increased process margins in gate etching with very thin gate dielectrics due to the relaxed over-etch requirements ▶

timeline

ATDF Highlights

Q2 • Installation and qualification of a full-field 193 nm scanner from Silicon Valley Group (SVG) and a Dianippon Screen (DNS)SK-2000 state-of-the-art track (SVG – Q2) (DNS – Q3) • Improved oxide dual damascene capability

Q3 • Just-in-time line loading • Implementation of a Shallow Trench Isolation (STI) process • Manufactureable 300 mm process developed in the ATDF; supported several member company 300 mm start-ups (Q3-Q4)

ATDF (continued)

- Improved oxide dual Damascene capability, providing a more stable comparison for experimental low-k processes

- Development of a disposable nitride spacer process. This enables ISMT to evaluate innovative LDD (lightly doped drain) source/drain extension processes

- Demonstration of chemical planarization of copper on low-k films, which previously delaminated under the mechanical force of the industry standard CMP techniques

A phased conversion of the ATDF to 300 mm will begin in 2001. In November, the Board of Directors approved the first phase of the conversion, which focuses on improvements in wafer processing to support tool evaluations for member company projects and the first 300 mm programs in low-k and copper.

In preparing to convert the ISMT's fab to 300 mm over the next three to four years, the ATDF has identified the key tools required for members to use for the high-volume production of 300 mm wafers. To provide Interconnect and FEP with 100 nm baseline wafer processing capabilities, for instance, the ATDF will need approximately one hundred 300 mm tools. The strategy is to convert one technical division at a time from 200 mm to 300 mm, starting with Interconnect.

Transferring ATDF research activities to 300 mm will enable the ISMT programs to develop next-generation technologies on the most advanced state-of-the-art tool sets available. The ATDF will retain some 200 mm capability for several years to maintain compatibility with university research programs. The 300 mm transition will strengthen the ATDF's overall development capabilities. "A very strong ATDF will guarantee a strong future, both for our member companies and for the industry as well," said Dan Holladay, associate ATDF director.

In addition, a pilot program in the ATDF beginning in 2001 will provide supplier rooms adjacent to the fab. The program is designed so that equipment makers can perform tool tests in a secure and confidential area, yet still work jointly with ISMT on advanced films and process developments. ■

(**above**)
This Dainippon Screen SK-2000 advanced coater/developer track, linked to an SVG Micrascan 193, International SEMATECH's first full-field 193 nm scanner for resist and reticle development, extended feature resolutions to <130 nm, providing features at the 100 nm node and beyond.

(**above**)
Manufacturing technicians at work inside the ATDF.

(**above**)
The SEZ Spin-Processor 203 provides Copper contamination control by cleaning the back surface of wafers. This cleaning allows the wafers to be processed more effectively by other tools, improving cycle time.

Q4 • 50–67 percent cycle time improvement • 130 nm node capability established in the ATDF with new 193 nm technology • 24 x 7 program developed for a January 5, 2001 implementation

Sharing in Success

"defines the standard for collaborative, pre-competitive research"

"played a central role in defining...protocol"

"unique opportunity for member companies to review together common quality philosophies and methods"

"very valuable...in assessing and developing key technologies for our industry"

Thirteen member companies choose to belong to International SEMATECH (ISMT) for a multitude of reasons—many of which are shared across the membership, some of which are specific to each individual member company. In general, members find value in International SEMATECH's ability to:

- Coordinate the pre-competitive sharing of ideas and knowledge
- Accelerate technology development and share the costs
- Support key infrastructure deficiencies
- Provide a forum for networking and benchmarking
- Reduce risk by building consensus across the industry

The fact that over 91 percent of year 2000 milestones and deliverables were met (against a target of 85 percent) and that the divisions scored well on the Program Assessment Surveys (PAS), reaffirms the members' general satisfaction with the program set, but a true assessment of ISMT's value to members must also focus on individual success stories for each member company. Here are the comments from six member company technologists on a few such successes.

Front End Processes Research Center

"The Front End Processes Research Center, a joint development effort between International SEMATECH, the Semiconductor Research Corporation (SRC), and nine universities, now defines the standard for collaborative, pre-competitive research in the semiconductor industry. Launched to address the myriad of issues surrounding transistor fabrication below the 100 nm node, this cooperative effort is dealing with one of the greatest challenges facing the industry. The Center continues to make good progress on exceedingly difficult tasks: an excellent example is the work done to identify and screen future gate dielectrics and electrodes. The access to universities and the breadth of tools and processes that the Research Center provides are an exceptional value proposition to AMD. AMD factors the results of this effort into our technology development roadmap."

David Bennett
Technology Transfer Manager,
AMD

Equipment Improvement Productivity Teams (EPITs)

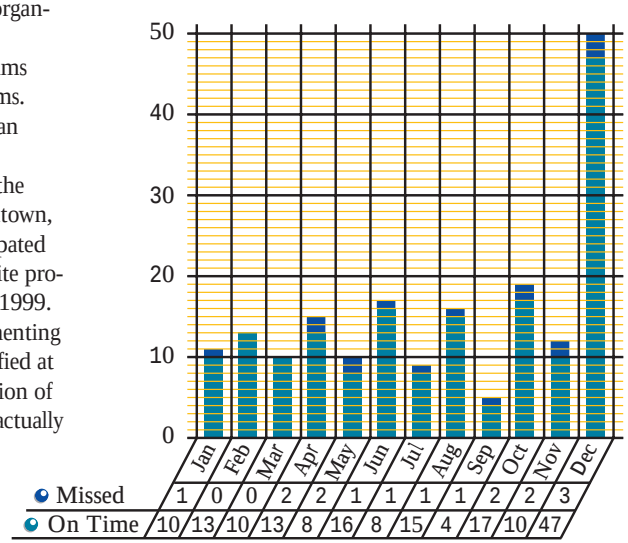
"This past year, Agere Systems saw a significant improvement in understanding the value received from the Equipment Productivity Teams—known as EPITs. International SEMATECH runs effective EPITs programs and meetings, but up until this year Agere did not fully capitalize on the benefit we knew existed. In 2000, we reorganized our approach to EPITs, tracking the implementation of existing EPITs programs and taking part in more beta-site programs.

Changes we made included having an Agere assignee in the EPITs program at International SEMATECH throughout the year. Last year, all of our facilities—Allentown, Reading, Orlando, and Madrid—participated in the International SEMATECH beta site program, greatly improving our return over 1999. We also put in place a process for documenting equipment improvement projects, identified at the EPITs meetings, through the generation of uniform trip reports. We track if we are actually performing the changes identified in those trip reports, and if so, we track any benefits from those changes, such as reduced maintenance time and improved yields. This improved approach has allowed Agere to take fuller advantage of International SEMATECH's EPITs program and see an improvement in our value received/cost ratio."

David Ojeda
EPITs Managers Working Group Member,
Agere Systems
(formerly Lucent Microelectronics Group)

Resists: 193 nm Benchmarking and 157 nm Feasibility

"International SEMATECH's 193 nm resist benchmarking project was very helpful to Hyundai Electronics. To meet our goal of obtaining 100 nm design rule devices, we tested several of the resists evaluated in International SEMATECH's project, selected four of them, and got good results; we are now making ▶



(**right**)
ISMT met over 91% of year 2000 milestones and deliverables, against an aggressive goal of 85%—the highest level ever achieved by the consortium.

Member Value (continued)

devices using these resist materials.

The 157 nm resist benchmarking work at International SEMATECH also gave us good information. Through ISMT, we had visibility into the current progress in 157 nm resist, and could see that absorption of polymers was not good enough to obtain good patterns. So we developed a new process called the 'amine gradient process' (AGP) that can be adjusted to the resist which has a moderate light absorption. We now have a plan to check out the 157 nm resist performance of benchmarked polymers using our AGP process. Hyundai has partnered actively with International SEMATECH and Grant Willson's research group at The University of Texas to make significant contributions to the research in this important area."

Jae-Chang Jung
Senior Member of Technical Staff,
Manager, Hyundai Electronics

157 nm Reticle Handling

"157 nm lithography will play a critical role in the definition of small feature sizes at the 70 nm technology node. The implementation of this lithography generation will require the timely integration of exposure tools, photoresist, and mask making into production-worthy technologies.

The International SEMATECH reticle handling working group played a central role in defining the 157 nm reticle handling protocol. One of the most important achievements of this group was to define a protocol which is independent of the selection of pellicle material. This allows the mask making suppliers and exposure tool manufacturers to design high-volume manufacturing tools without the constraints of nitrogen purged carriers. It also allows the industry the development time to optimize the selection of the pellicle material."

Gerald Marcyk
Director, Components Research,
Intel Corporation

Quality Council

"The Quality Council, as established and fostered by International SEMATECH, offers a unique opportunity for member companies to review together common quality philosophies and methods across the industry. Because of the broad, high-level representation and experience on the Council, it is a very efficient forum to determine if a common relevancy or consensus exists in the industry on a given topic. The Quality Council operates at a 'pre-competitive' level, which allows even competitors to work together in raising common standards and performance levels in the marketplace. Focus topics have included greater understanding of customer expectations and perceptions; how we can better communicate with industry suppliers about our common needs; the general directions of quality philosophies and methods; addressing common industry challenges in failure analysis and reliability technologies; and working together with a common voice to guide and influence the continuous improvements of such standards as ISO and QS.

An additional value-added aspect of the Quality Council is the fact that its membership has a broad international representation. Since customer needs are often different from country to country, sharing of best practices within the Council allows members to arrive at better approaches to serve their customers around the world. The openness and common respect of basic rules from all the participants allow the members to talk, share, and learn without encroachment on the competitive relationships in the marketplace. In this respect, we consider the Council's spirit and ethical standards to be a 'pillar of the community.' ST is benefiting greatly from its participation in the International SEMATECH Quality Council, and believes this membership will continue to be one of our important interfaces within the industry and marketplace."

Bob Banks
Vice President,
Quality Americas
Robert Sangy
Corporate Quality Director.
STMicroelectronics

Copper and Low-k

"The Interconnect Group at International SEMATECH has been very valuable to TI in assessing and developing key technologies for our industry. TI has incorporated International SEMATECH's early learning into our R&D processes and business plan, and has staffed the Interconnect group with some of TI's best technical talent. This has been a very successful and rewarding strategy for TI, particularly in terms of copper barriers, low-k materials benchmarking and characterization, and copper/low-k integration approaches."

JD Luttmer
Interconnect Department Manager,
Texas Instruments ■

suppliers

Establishing New Initiatives in Supplier Relations

(**above L-R**)
Neil Gayle,
Program Manager,
Supplier Relations
Chris Daverse,
Manager,
Supplier Relations

(**above**)
Dave Anderson,
Director,
Supplier Relations

Supplier Relations has always been at the heart of International SEMATECH (ISMT); from its inception, the consortium's success has been inextricably linked with the quality of its partnerships with the supplier community. To realize the Roadmap, both sectors of the industry—device-makers and equipment and materials suppliers—must cooperate more closely than ever before. "New times create new challenges," stated Dave Anderson, director of Supplier Relations. "The dynamic changes we've seen in the industry over the last few years—the expanding global market, the accelerating technology roadmap, the deepening of traditional industry cycles, the consolidation that is taking place within the industry, the expansion of suppliers' capabilities into areas such as process development and integration—have called for new initiatives in International SEMATECH's relations with the global supplier community."

The objectives of the Supplier Relations program are to support all ISMT interactions with global suppliers, to maintain a healthy, competitive, and globally diverse equipment supplier industry; to demonstrate the value of International SEMATECH to suppliers; to fully understand supplier concerns; and to build relationships with suppliers and supplier organizations. The key to achieving these objectives is clear and open communication, followed by appropriate action. This year the Supplier Relations division, led by Anderson, listened carefully to the supplier community on issues they experience in dealing with consortia—such as cost share, intellectual property protection, and the "fish-bowl" effect—and on the larger business and economic issues related to the accelerating Roadmap and the uncertainty of multiple technology development paths. ISMT responded with a series of innovative actions and programs.

Industry Executive Forum

In the most visible example of fostering communication and appropriate action, ISMT hosted three Industry Executive Forum (IEF) meetings during the year in conjunction with regular meetings of its Board of Directors. International SEMATECH brought together senior executives representing 18 supplier companies, 16 device manufacturers, and six consortia or associations from around the world to engage in informal and interactive discussions of key economic, business, and technical challenges facing the global semiconductor industry. Together, customers and suppliers addressed such critical topics as how the industry can best realize the *International Technology Roadmap for Semiconductors* (ITRS) given timing requirements, technology challenges, and available resources; how supply chain cycle time can be improved; and what steps the industry can take to manage and predict business cycles in order to minimize the risks of downturns.

These discussions generated several cooperative efforts—a survey on the top issues impacting equipment lead times, reports on the feasibility of joint action in the areas of long-lead inventory items and base model tools, a review of 300 mm equipment standards, and new refinements to the industry economic model. Moreover, as a result of discussion during the April IEF, International SEMATECH launched an e-Diagnostics program to help guide standards for this emerging maintenance tool. By July the program had attracted participation from a host of different suppliers and had already published an initial set of standards guidelines. Progress continues on this important program, with active engagement from both device makers and suppliers—a stellar example of the benefits of working together on a common industry challenge.

In a bold move in the second half of the year, the IEF participants agreed in principle to move from words to action by defining joint programs to implement some of the powerful ideas that have come from the IEF discussion forums, starting with the challenge of mitigating industry cycles. In the April 2001 meeting, the IEF will review proposals and determine the appropriate mechanism and methodology for joint pre-competitive programs. "In addition to providing a high-level, global forum for discussion of key industry challenges," said Anderson, who directs and chairs the IEF sessions, "we're now looking at ways in which, for the first time, suppliers and device makers will jointly and formally take action to address some of those challenges. Our industry is on the verge of making history with this unprecedented level of customer-supplier cooperation."

Strategic Partnerships and Infrastructure Initiatives

While the IEF addressed the larger business and economic issues facing the industry, International SEMATECH also worked on ▶

Suppliers (continued)

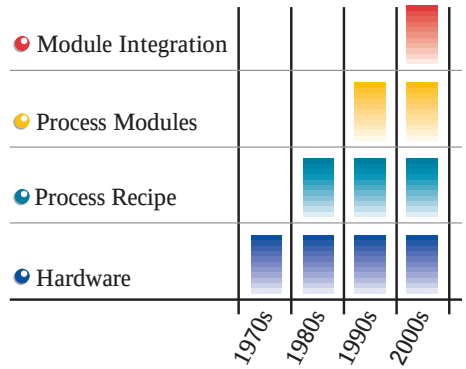
other levels as well to communicate and coordinate effectively with the supplier community. Targeted supplier workshops were held in support of ISMT programs on economic modeling, capital productivity, and e-Diagnostics, with active supplier participation. During 2000, International SEMATECH forged an even stronger partnership with the global supplier organization Semiconductor Equipment and Materials International (SEMI), well known throughout the industry for its trade shows, conferences, and training programs. ISMT looks forward to working closely with SEMI in coordinating joint programs coming out of the IEF initiative.

In a series of executive reviews with over a dozen global equipment suppliers deemed most critical to our members, ISMT's senior leadership met with executives and technologists from each company to share strategic direction, compare and coordinate technology roadmaps, and identify mutually beneficial areas for interaction. "The executive reviews are a key element in forging strategic partnerships with the supplier community," said Chris Daverse, Supplier Relations manager. "Nothing replaces the value of face-to-face dialogue as we seek to understand one another, build relationships, and ultimately work together to meet the needs of the industry at large."

Behind the scenes, ISMT's Supplier Relations Division worked hard with the other divisions and the Advanced Technology Development Facility (ATDF) to maximize the value suppliers receive from interactions with ISMT by streamlining the contracting and procurement process, revisiting intellectual property and publication policies, aligning executive-level agreements with working-level technical execution, and encouraging innovative reciprocal relationships.

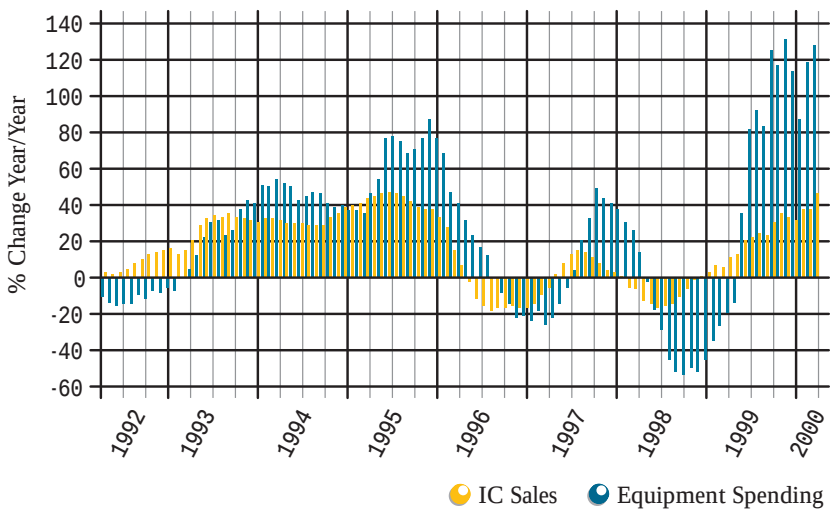
"International SEMATECH has historically worked with suppliers in tool development and improvement," stated Neil Gayle, Supplier Relations program manager. "As the pace of market-driven applications continues to accelerate the need for technology solutions, our goal is to expand this traditional relationship, and to find new ways to partner with suppliers in technology and infrastructure programs that offer a clear 'win' to both the supplier and the consortium." As of the end of 2000, one such win-win initiative was underway—a pilot study for the concept of private supplier rooms at International SEMATECH to counter the concern over "fish-bowl," or open visibility at early stages of tool development. ■

Evolving Role of Equipment Suppliers



(left)
The Industry Executive Forums sponsored by ISMT have engaged senior chipmaker and supplier executives in discussions about what steps the semiconductor industry can take to manage and mitigate the effects of business cycles.

Supply Chain Dynamics



(left)
Among the dynamic changes in the industry over the last few years is the expansion of suppliers' capabilities into areas such as process development and integration.

assignees

Making Connections, Delivering Technology

"Come work with us and meet the world." At International SEMATECH (ISMT), that's more than just a slogan. With 13 member companies representing some of the world's largest semiconductor manufacturers, ISMT assignees work with individuals from all around the globe.

Approximately 60% of the technical positions at the consortium are staffed by assignees from member companies, working at all levels of the organization. Typically, assignments vary in duration from one to three years.

"The assignee program is considered one of the top sources of return on investment for our members," said Sean Murphy, staffing manager. "But just as important is the value the assignee gains from the experience."

Since the program operates on a rotational basis, there are always assignees in various stages of their assignments at ISMT. For some, the assignment represents a career move; for others it offers an opportunity for a new lifestyle. For all, the assignment represents the chance to affect the future of the industry.

Orientation

TSMC assignees C.C. Lin and Dah-Chung Oye-Yang won't soon forget the meaning of the term *orientation*. The young newlyweds had barely begun their new life together when they came to ISMT, thousands of miles away from their friends and families, their jobs, and all that was familiar to them in Taiwan.

Their dual assignments, which began in March of 2000, brought the couple to the U.S. for the first time. Determined not to let language or cultural differences encumber them, both quickly learned English with the aid of a pocket translator and a self-paced computer-based language learning software program.

In addition to settling into their new life together in Austin, the two embarked on new career directions at ISMT. As a former manufacturing engineer at TSMC, Lin finds his position at ISMT as a project manager in mask defect printability extremely challenging. "Alternative phase shift masks is still a relatively new process at TSMC. Evaluating the use of this type of mask helps in our understanding and application of this technology," he said.

Owe-Yang also enjoys the challenges and rewards that the work at a research and development facility brings. As a lithography engineer responsible for the baseline process for the 157 nm Exitech microexposure tool, her work involves determining a set of optimum photoresist processing conditions that will result in a daily qualifying procedure in the fab. "Much guesswork is involved," she said, "which makes the work very interesting." But ultimately, she says, the knowledge gained is the reward.

Early Assignment

Adaptation comes relatively easy for Philips assignee Steve Smith. In the past 17 years, his career with Philips has taken Smith's family to Orem, UT; Albuquerque, NM; Austin, TX; and ultimately, a planned move to France when his assignment is complete.

Smith was encouraged to look into the assignee program by two co-workers, both current ISMT assignees. "I'd read about International SEMATECH in technical journals and had attended some International SEMATECH conferences, so I was already familiar with some of the work done here." When he heard of an assignee opportunity, Smith jumped at the chance. "I was eager to learn and be a part of the future state-of-the-art technology," he said.

His work in the Interconnect Division keeps him directly involved in future technology. As project manager for Advanced Barriers, Smith characterizes and analyzes the thin film properties and electrical characteristics of devices to help develop equipment for a technology still two to five years out. "This is really an emerging technology—still in its infancy—one which will enable the industry to achieve the shift from the 100 nm to the 70 nm node as outlined in the ITRS," he said.

Using what he calls "really neat science," Smith also works in the area of thin-film metrology, establishing the best method for measuring copper voids. "In effect, we're counting atoms," he said of his work to improve manufacturability and efficiency.

The assignment experience is above and beyond what Smith ever expected. "What's great about this organization is that you interface and integrate with other groups, which is conducive to success for all," he said. Smith ▶

Assignees (continued)

looks forward to the remainder of his assignment with even higher expectations. "The outcome here has great technological impact. My work here is really a design on the future—a future vision."

Midpoint

At the midpoint of his assignment, 14-year Infineon veteran Eric Graetz's primary efforts were focused on the efficient transfer of information and technology back to his member company. This constant exchange of information and reports, as well as four trips home during the year, enabled him to expand on a well-developed receivership structure within Infineon. Much of his time during these trips was spent meeting with groups working on particular issues, as well as one-on-one meetings with engineers and design engineers. "My job is to involve more engineers back home, and transfer the knowledge of processes and problems so they know what to look for," he said.

Graetz's responsibility as the Doping Development project leader has given him a hand in shaping future technologies. "Our challenge is to overcome the physical barriers of shrinking devices, which is critical. Otherwise we will not meet the increasing device speed requirements," he said.

Graetz also feels that his day-to-day involvement in business and processes at ISMT delivers Infineon more insight into the diverse semiconductor industry. And, since many of ISMT's projects are also within the Infineon roadmap, Graetz added, costly duplicated efforts can be avoided.

Late Assignment

The end of the year also marked the end of STMicroelectronics' Olivier Louveau's assignment at ISMT. As an Etch project engineer in the Advanced Technology Development Facility (ATDF), Louveau's work in ISMT's Tool Application Program (TAP) was instrumental in providing suppliers with the necessary information and data to improve their tools to meet customer and industry needs.

"My objectives were quite clear—to provide the most up-to-date information to further 300 mm efforts for STMicroelectronics and the industry altogether," says Louveau. In turn, he notes, all ISMT member companies will have wider choices when it comes to 300 mm tools.

Although Louveau's excitement about returning to his family in Crolles, France was readily apparent, the conclusion of his assignment was also met with a measure of regret, as his project will be completed in early 2001 without him. "But with good results," he added. The experience he gained at ISMT, however, has left him suited for a similar R&D position upon his return to STMicroelectronics. "I've learned a lot about the industry related to process and management, through other people and other places."

Return to Member Company

"Expect and accept differences" is the advice former Intel assignee Ed Muzio offers incoming assignees. "Be open minded, and you'll do just fine." For Muzio, the task versus relationship balance was the most significant difference between his previous work at an Intel production facility and his assignment at the consortium.

Ironically, that is exactly what prepared the former ISMT Lithography project manager for his new position upon returning to Intel in 2000. The relationship management skills required to organize and structure an industry-wide program in Reticle Handling with world-wide participation were "an obvious advantage," says Muzio of his ISMT experience and the role it played in acquiring his new position as Intel's Rotation Engineer Program manager.

"The nature of my assignment certainly advanced my project management skills," said Muzio. Frequent one-on-one meetings with Intel matrix managers and internal R&D, as well as high-level on-site presentations about his work at ISMT demanded these skills.

But the highlight of his assignment, Muzio said, was the ISMT volunteer experience that enlightened him about the farther-reaching impacts of organizational effectiveness. He left behind a valuable legacy in the successful TLC (Teaching, Learning, Caring) program, which he re-developed to teach pregnant and parenting teens the essential learning and decision-making skills to succeed in an adult world. ■

(**left L-R**)
C.C. Lin and Dah-Chung Owe-Yang, TSMC
Steve Smith, Philips
Eric Graetz, Infineon
Olivier Louveau, STMicroelectronics
Ed Muzio, Intel

support services

Support Services: Assuring Effectiveness and Efficiency

Managing business processes in a groundbreaking global consortium and in a fast-paced industry demands bold innovation and constant fine-tuning. All of the consortium's support functions launched new initiatives to maximize effectiveness and streamline the cost of doing business; several of those initiatives drew special praise from our members.

Clear, consistent and universally-accepted business processes are at the heart of our consortium. Under the leadership of director Tom Bowers, the Account Management group formed cross-functional teams to clarify and improve processes in three key areas: budget decision-making and reporting, advisory group structure and project assessment surveys. The teams researched these issues and presented detailed recommendations to the Executive Steering Council (ESC) for approval. "Our teams came up with solutions that all thirteen member companies wholeheartedly support. We're now making sure the new procedures are implemented and institutionalized throughout International SEMATECH," said Bowers.

Carri Crowe, in Development Contracts, first heard on May 8 about International SEMATECH's (ISMT's) proposed partnership with the Belgian research institute IMEC in gate stack/high-k development. From that day until July 20, when the last details were finalized, her life was consumed by the supercharged effort to get an agreement negotiated in time for signing at the July 27 Board of Directors meeting in Paris. Crowe worked with Bob Falstad, General Counsel, on the contract's terms and conditions, while Mike Jackson and Ed Strickland in Front End Processes developed the technical statement of work.

"Designing a partnership agreement between two strong organizations with very different operational models called for a high level of trust, a commitment to fairness, and a lot of hard work on both sides," stated Crowe. The teams worked through tough issues involving intellectual property, assignees, and even governing law before ultimately completing the agreement on time and on target. Both the Executive Steering Council (ESC) and the Board of Directors paid tribute to this achievement, and Crowe appreciated the learning experience, since her next challenge was to negotiate a similarly complicated agreement with the German Fraunhofer Institutes.

Use of the secure member company web site has continued to climb over the last twelve months, reported Robert Noland, Strategic Development manager in Information Technology. "Hits on the site have increased by a factor of ten, to about 20,000 per month, over 4,000 users have set up accounts, information is being updated daily, and the site now holds about 13,000 ISMT publications," he said. These numbers speak to improvements in features, response time, maintenance, and training, as the secure web site team continues to remove time and space barriers to link the ISMT community together. In 2001, new modules will add even more capabilities such as favorite links, threaded discussion groups, and on-line meeting registration.

In an Advanced Technology Development Facility (ATDF) October review, financial planners Stuart Clark and Chuck Fry won kudos from ESC Chairman Bill Rozich and other members of the ESC's ATDF subcommittee for the "most comprehensive and clear" set of financial reports they have yet seen on the facility. The reports were the visible representation of a behind-the-scenes team effort dedicated to the best possible financial oversight of the ATDF. Clark cites several success factors: a close working relationship between the Finance team and ATDF leadership; a new effort to consolidate all capital activity at ISMT; constructive guidance from the ESC subcommittee and the ATDF team; and an improved cost model developed by a cross-functional group from Finance, Information Technology, and the ATDF. "Simply stated, the reports are good because the people are performing well, and because we're all committed to continuous improvement," said Clark. ■

(**left L-R**)
Carri Crowe, Contract Manager
Robert Noland, Strategic Development Manager
Tom Bowers, Director of Account Management
Stuart Clark, Financial Planner

community

Reaching Out to Help Others

International SEMATECH (ISMT) is committed to strengthening our community. We are proud that year after year our employees lead the way in this effort by sharing their time and their talents in community projects.

In 2000, our volunteers forged exciting new territory, working with our neighbors at Allison Elementary School. With our first Books-for-a-Buck sale, we raised more than $500 to help support the school's Reading Is Fundamental (RIF) program. "The book sale was a unique event in which International SEMATECH employees both donated and purchased the books to raise money for RIF," said ISMT Community Relations Manager Christie Cochren. "We took the opportunity to educate our employees about children's literacy, raising the awareness of programs like RIF and emphasizing the role we all play in this effort."

Other activities rely on the talents of our employees, such as Project Linus, a nationwide organization that provides blankets to children facing substantial distress in their lives. In a week's time, a group of International SEMATECH volunteers stitched, sewed and quilted a total of 75 homemade security blankets for Project Linus. With a modest amount of money donated by International SEMATECH for materials, these seamstresses contributed their special talents during lunch breaks, and before and after work to help provide comfort for children at Austin's Brackenridge Children's Hospital and the Neonatal Intensive Care Unit at The Children's Hospital of Austin.

We recognize that corporate donations play a role in supporting our community, and in 2000 we had the pleasure to see one of our donations multiply beyond our expectations. A $1,500 donation, initially provided by ISMT in the fall of 1999 to stock Del Valle Junior High's Kids-to-Kids Supply Store, eventually returned an $8,000 contribution to UNICEF by the end of the school year in 2000 through the efforts of the students at Del Valle. By purchasing supplies with the seed money and reselling those supplies to fellow students, the Supply Store workers generated a substantial profit. "This project was recognized by UNICEF as being a potential model for other schools to follow in fund-raising efforts," said Cochren. "The purpose was to teach students how to run a small business, to demonstrate that they can make a difference in the lives of others through their contributions to UNICEF, and to bring business education into the classroom. And, as one can see, it was a raving success."

We concluded the year with our annual support of the Brown Santa program sponsored by the Travis County Sheriff's Department, which provides gifts and food to families in the Austin area during the Christmas holidays. ISMT employees raised more than $3,920 throughout the year to help the program. In conjunction with the Del Valle ISD Teaching, Learning, and Caring Program (TLC), International SEMATECH volunteers and TLC participants also donated 45 hours of their time to wrap and package Brown Santa gifts. Through the TLC, ISMT volunteers teach life skills based on Stephen Covey's work on the *Seven Habits of Highly Effective Teens* to 50 pregnant and parenting teens.

"As corporate citizens, we realize that we get out of the community what we put into it," said International SEMATECH President and CEO, Mark Melliar-Smith. "International SEMATECH is especially proud of our employees' efforts to make a significant contribution to the local community." ■

Below (right L-R)

Linda Cline, director's assistant in Human Resources, holds up a handmade security blanket made by volunteers to donate to Project Linus.

Nancy Paine, service contracts coordinator, browses through a book donated for the Books-for-a-Buck sale which raised money for the Allison Elementary School Reading Is Fundamental (RIF) Program.

Christie Cochren (left), ISMT community programs manager, stands with UNICEF representative Nicole O'Neil (right) as an $8,000 check is presented to UNICEF on behalf of the Del Valle Junior High Kids-to-Kids School Store, for which International SEMATECH provided the seed money.

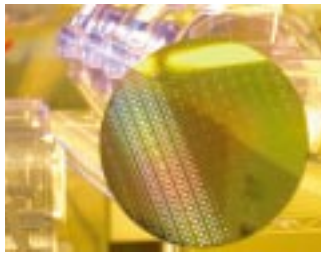
bod/esc

Board of Directors/ESC

International SEMATECH
Board of Directors
- Chairman
  - William J. Spencer *(January - April)*
  - OB Bilous *(May - December)*
- AMD
  - Bill Siegle
  - Gary Heerssen *(Alternate)*
- Conexant
  - Terry Ellis
  - Dwight W. Decker *(Alternate)*
- Hewlett-Packard
  - Sam Angelos
- Hyundai
  - Sea Chung Kim
  - Hee-Koo Yoon *(Alternate)*
- IBM
  - Harry C. Calhoun
  - John DiToro *(Alternate)*
- Infineon
  - Wilhelm Beinvogl
  - Johann Harter *(Alternate)*
- Intel
  - Michael R. Splinter
  - Jai Hakhu *(Alternate)*
- International SEMATECH
  - OB Bilous
  - William J. (Bill) Spencer
  - C. Mark Melliar-Smith
- Lucent
  - Dave Williams
  - Paul Mostek *(Alternate)*
- Motorola
  - Bill Walker
  - Gregg Bartlett *(Alternate)*
- Philips
  - Stuart K. McIntosh
  - T.A.C.M. (Theo) Claasen *(Alternate)*
- Semiconductor Research Corporation (SRC)
  - Larry W. Sumney
- STMicroelectronics
  - Joel Monnier
  - Michel Montier *(Alternate)*
- TSMC
  - F.C. Tseng *(Jan-Mar)*
  - Rick L. Tsai *(Apr-Dec)*
  - Shang-Yi Chiang *(Alternate)*
- Texas Instruments
  - Yoshio Nishi
  - K. Bala *(Alternate)*

International SEMATECH
Executive Steering Council (ESC)
- AMD
  - David Bennett
  - David Kyser *(Alternate)*
- Conexant
  - Lee LJ Chung
- Hewlett-Packard
  - Don Barton
  - James McMahon *(Alternate)*
- Hyundai Electronics
  - Heung-Lak (HL) Park
  - Ki-Ho Baik *(Alternate)*
- IBM
  - Bill Rozich, *ESC Chairman*
  - Joseph G. Nemeth *(Alternate)*
  - Jeff Robinson *(Alternate)*
- Infineon
  - Peter Kuecher
  - Juergen Ruestig *(Alternate)*
- Intel
  - Paolo Gargini
  - Michael J. Ryan *(Alternate)*
- International SEMATECH
  - Rinn Cleavelin
  - Tom Bowers
- Lucent
  - Dale Ibbotson
  - Gladys Felton-Upton *(Alternate)*
- Motorola
  - Sean Hunkler
  - Elizabeth J. Weitzman *(Alternate)*
- Philips
  - Alfred J. (Fred) van Roosmalen, *ESC Vice-Chairman*
- Semiconductor Research Corporation (SRC)
  - Dinesh Mehta
- STMicroelectronics
  - Michel Montier
  - Herve Mingam *(Alternate)*
- TSMC
  - C.C. Wei
  - Mong-Song Liang *(Alternate)*
- Texas Instruments
  - C. Robert (Bob) Helms
  - Allen Bowling *(Alternate)* ■

2000 International SEMATECH Program Advisory Groups (PAGS)



Environment Safety and Health PAG

AMD
- Reed M. Content, *Alternate*
- Klaus Haupold, *Alternate*
- Michael May, *Primary*
- Don McIntosh, *Alternate*

Conexant
- Michael S. Gooch, *Primary*
- Eric Moschet, *Alternate*

Hewlett-Packard
- Sharon Pleu, *Primary*
- Debbie Sibert, *Alternate*

Hyundai
- Heung-Sik Kwak, *Primary*
- Kee-Joon Oh, *Alternate*
- Sam Pakdel, *Alternate*

IBM
- Jay M. Dietrich, *Primary*
- Thomas Tamayo, *Alternate*

Infineon
- Wolfgang Bloch, *Primary*

Intel
- David Harman, *Alternate*
- James Jewett, *Primary*
- Richard Parker, *Alternate*

Lucent
- Theodore D. Polakowski, *Primary*
- Mark Mitchell, *Alternate*

Motorola
- Sarah Gibson, *Primary*
- Laura A. Mendicino, *Alternate*

Philips
- Leo Klerks, *Primary*

Semiconductor Industry Association (SIA)
- Chuck Fraust, *Primary*

STMicroelectronics
- Fabio Borri, *Alternate*
- Maurizio Micale, *Alternate*
- Alain Roche, *Primary*
- Jeffrey Sczechowski, *Alternate*

Texas Instruments
- Coleen C. Miller, *Alternate*
- Timothy Wooldridge, *Alternate*
- Tim Yeakley, Primary

TSMC
- Jim Chen, *Alternate*
- Jung-Shen Hsiue, *Primary*
- Middle Huang, *Alternate*

U.S. Department of Defense
- Jeffrey D. Williams, *Primary*

Front End Processes PAG

AMD
- Mark I. Gardner, *Alternate*
- Jeff Haines, *Alterenate*
- Robert B. Ogle, *Primary*

Conexant
- Aniruddha B. Joshi, *Primary*
- Marie Luo, *Alternate*

Hewlett-Packard
- John Compton, *Primary*

Hyundai
- Jin-Won Park

IBM Corporation
- Susan L. Cohen, *Alternate*
- Stephen Fox, *Alternate*
- Michael Jackson, *Chair*
- James S. Nakos, *Primary*

Infineon
- Christine Dehm
- Reinhard Mahnkopf, *Alternate*
- Thomas Schiml, *Alternate*

Intel
- Maciek E. Orczyk, *Alternate*
- Jon S. Owyang, *Primary*

Lucent
- Gregg S. Higashi, *Primary*

Motorola
- Steve Anderson, *Primary*

Philips
- Carel J. van der Poel, *Primary*

STMicroelectronics
- Jean Galvier, *Primary*
- Herve Mingam, *Alternate*
- Mauro Alessandri, *Alternate*

Texas Instruments
- Stephanie W. Butler, *Primary*
- Luigi Colombo, *Alternate*
- Rick Wise, *Alternate*

TSMC
- Wei-Kun Yeh, *Alternate*
- K.L. Young, *Primary*

Lithography PAG

AMD
- Paul W. Ackmann, *Alternate*
- Chris Lyons, *Primary*

Conexant
- Nandasiri Samarakone, *Primary*

Hewlett-Packard
- Valerie Bach, *Primary*

Hyundai
- Chang-Nam Ahn, *Primary*
- Cheol-Kyu Bok, *Alternate*
- Ki-Ho Baik

IBM
- Timothy R. Farrell, *Primary*

Infineon
- Guenther Czech, *Primary*
- Wolf-Dieter Domke, *Alternate*

Intel
- Janice M. Golda, *Primary*
- Peter J. Silverman, *Alternate*

Lucent
- Jim Blatchford
- Om Nalamasu
- Anthony E. Novembre, *Alternate*
- Thomas M. Wolf, *Primary*

Motorola
- Victor Pol, *Alternate*
- Bernard J. Roman, *Primary*

Philips
- Jan-Willem Gemmink, *Alternate*
- M.W.M. Graef, *Primary*
- Casper Juffermans, *Alternate*

STMicroelectronics
- Jean Massin, *Alternate*
- Paolo Canestrari, *Primary*
- Daniel Henry, *Primary*
- Dominique Labrunye, *Alternate*

Texas Instruments
- Maureen A. Hanratty, *Primary*
- Michael F. Pas, *Alternate*

TSMC
- Kuei-Wu Huang, *Alternate*
- Yao-Ching Ku, *Alternate*
- Anthony Yen, *Primary*

Multilevel Metals PAG

AMD
- William Brennan, *Primary*
- Richard J. Huang, *Alternate*
- John A. Iacoponi, *Co-Chair*

Conexant
- Maureen Brongo, *Alternate*
- James F. Fraser, *Alternate*
- Bin Zhao, *Primary*

Hewlett-Packard
- Gary Castleman, *Alternate*
- Tim Koch, *Primary*

Hyundai
- Jin-Woong Kim, *Alternate*
- Sibum Kim, *Alternate*
- Yil-Wook Kim, *Alternate*
- Jeong-Gun Lee
- Heung-Lak Park, *Primary*

IBM
- Janos Havas, *Alternate*
- Stephen Luce, *Primary*

Infineon
- Hans-Joachim Barth, *Primary*
- Reinhard Mahnkopf, *Alternate*
- R.J. Schutz, *Alternate*

Intel
- Melton Bost, *Primary*
- Carolin Seward, *Primary*

Lucent
- Richardson Adebanjo, *Alternate*
- Ruichen Liu, *Alternate*
- Susan C. Vitkavage, *Primary*

Motorola
- Matthew T. Herrick, *Primary*
- Bradley M. Melnick, *Alternate*
- Ruben B. Montez, *Alternate*
- Cindy Simpson
- Paul Winebarger, *Chair*

Philips
- Teus Brand
- Miguel Delgado, *Alternate*
- Dirk Gravesteijn, *Primary*

SISA
- Michael F. McGraw, *Primary*

Texas Instruments
- J.D. Luttmer, *Primary*
- Andrew J. McKerrow, *Alternate*
- Gregory B. Shinn, *Alternate*
- Kelly J. Taylor, *Alternate*
- Stephen P. Zuhoski, *Alternate* ▶

Note: *The people listed held membership positions for all or part of 2000. Primary and alternate positions may have changed during the year.*

PAGS (continued)

TSMC
- Simon Lin, *Alternate*
- S.L. Shue, *Alternate*
- Ming-Hsing Tsai, *Alternate*
- Wei-Kun Yeh, *Alternate*
- Chen-Hua Yu, *Primary*

Manufacturing Methods and Productivity PAG

AMD
- Michael D. Brooks

Conexant
- Tony Martinez, *Primary*

Hewlett-Packard
- Don Barton, *Primary*

Hyundai
- Dong-Won Baik, *Primary*
- Seungil Kim, *Alternate*

IBM
- Scott Fullerton. *Primary*

Infineon
- Henry Becker

Intel
- Christopher J. McDonald, *Primary*
- Patricia A. McDonald, *Alternate*

International SEMATECH
- Scott S. Kramer
- Vernon E. Reynolds
- Michael Schwartz

Lucent
- Jerffry M. Neve

Motorola
- Chris Magnella

Philips
- W.J.M.J. Josquin

STMicroelectronics
- Edwin Dobson, *Primary*

Texas Instruments
- Judy B. Shaw

TSMC
- J.K. Wang

Metrology Yield Management PAG

AMD
- Iraj Emami, *Primary*
- William Funsten
- Richard W. Jarvis, *Alternate*
- David L. Jensen
- Michael McIntyre, *Alternate*
- James Pak
- Michael A. Retersdorf
- Bryan Tracy

Conexant
- Dennis L. Cerney, *Primary*
- Steven J. Keeler, *Alternate*
- George Parker, *Alternate*

Hewlett-Packard
- Tze-Yiu Yong, *Alternate*
- Owen W. Youngblood, *Primary*

Hyundai
- Bong-Ho Kim, *Alternate*
- Chul-Hong Kim, *Primary*

IBM
- John Colt
- William A. Fil, *Primary*
- Christopher W. Long
- Daniel N. Maynard
- Raymond J. Rosner
- Wanda Tomlinson, *Alternate*

Infineon
- Christine Dehm
- Peter Federl
- Hans Glawishnig
- Martin Gutsche
- Rudolf Laubmeier
- Ulrich Mantz
- Shoaib Zaidi

Intel
- Derek G. Fisher, *Primary*
- Laura Oliphant, *Primary*
- Dilip Patel

International SEMATECH
- Alain C. Diebold
- Firdousali Lakhani
- Tarun K. Parikh
- Norma Williams

Lucent
- Jeffrey B. Bindell, *Primary*
- Margarita Espino, *Alternate*
- Todd C. Henry
- Ronald L. Remke

Motorola
- Rick Cosway, *Alternate*
- Ted White, *Primary*

Oak Ridge National Laboratory
- Walter Gardner
- Kenneth W. Tobin
- Raymond W. Tucker
- Randall Wetherington

Philips
- Adolf Belka, *Primary*

Sleuthworks, Inc.
- Gary M. Scher

STMicroelectronics
- Patrick Dussouilez

Texas A&M University
- Duncan M. Walker

Texas Instruments
- Marylyn Bennett
- Daniel V. Grelinger, *Primary*
- Richard L. Guldi
- Dan Iversen, *Alternate*
- Robin Worley

TSMC
- King Lee
- Y.J. Mii
- Wei-Kun Yeh
- K.L. Young

University of Michigan
- James R. Moyne

Plasma Etch/Patterning PAG

AMD
- John R. Behnke
- Douglas (Doug) Bonser
- Mark S. Chang, *Primary*
- Marina Plat, *Alternate*
- Jeorg-Peter Weher

Conexant
- Viswanathan Ramanathan, *Primary*
- Bud Yung

Joe White

Hewlett-Packard
- Cathy Peltier

Hyundai
- Young-Mok Ham, *Alternate*
- Jin-Woong Kim, *Alternate*
- Sibum Kim
- Yilwook Kim
- Heung Park

IBM
- Michael Armacost, *Alternate*
- Timothy J. Dalton, *Primary*
- Rich Ferguson, *Primary*
- Aki Sekiguchi, *Alternate*
- Tom Weeks, *Primary*

Infineon
- Has-Joachim Barth, *Primary*
- Alois Gutmann, *Alternate*
- Alfred Kersch, *Alternate*
- Brian Lee, *Primary*
- Swami Mathad, *Alternate*

Intel
- Melton Bost, *Primary*
- Janice M. Golda, *Alternate*
- Mark Sandoval, *Primary*

International SEMATECH
- Gil Shelden, *Team Chair*

Lucent
- Anne Akerson, *Alternate*
- James Blatchford, *Alternate*
- Stephen W. Downey, *Alternate*
- Taeho Kook, *Primary*
- Avi Kornblit, *Alternate*
- Tseng-Chung (John) Lee, *Alternate*

Motorola
- Gerald Bernard, *Primary*
- Tom Lii, *Alternate*
- Lloyd C. Litt, *Primary*
- Victor Poi, *Primary*
- Paul Winebarger, *Primary*
- Wei Wu, *Alternate*

Philips
- Teus Brand, *Primary*
- Miguel Delgado, *Alternate*
- Jan-Willem Gemmink, *Primary*
- Dirk Gravesteijn, Alternate

STMicroelectronics
- Lucio Colombo, *Primary*
- Pierre-Jerome Goirand, *Primary*

Texas Instruments
- Robert Kraft, *Primary*
- James Laney
- Mikki Mikkilijneni
- Thomas W. (Tom) Lassiter

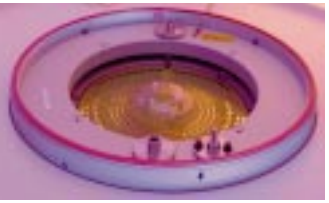
TSMC
- Le Chao, *Primary*
- Shih-Chang Chen, *Primary*
- S.M. Jang, *Primary*
- Mong-Song Liang
- H.J. Tao, *Primary*
- Chen-Hua Yu, *Primary* ■

Note: *The people listed held membership positions for all or part of 2000. Primary and alternate positions may have changed during the year.*

assignees

Assignees

AMD	
Lynn Armentrout	*Lithography*
Thomas Brown	*Interconnect*
Curtis Doss	*MM&P*
Amy Engbrecht	*ESH*
Clarence Ferguson	*Front End Processes*
Patricia Gabella	*Lithography*
Richard Jarvis	*ESH*
Deborah Riley	*Front End Processes*
Marlin Shopbell	*MM&P*
Jonathan Spurlock	*ATDF*
Sanjay Yedur	*Lithography*
Conexant	
Husam Alshareef	*Front End Processes*
Volker Blaschke	*Interconnect*
Jerry Brandewie	*Account Management*
Hsu-Yueh Chien	*Lithography*
Nishrin Kachwala	*Lithography*
Robert Sherman	*ATDF*
Hewlett-Packard	
Kenneth Vandehey	*MM&P*
Hyundai	
Chan Lim	*Front End Processes*
Chung-Soo Han	*MM&P*
Hyeong Soo Kim	*Lithography*
Ju-Hwan Kim	*Lithography*
Sangwook Kim	*ATDF*
Young-Sik Kim	*Lithography*
Hoe Seok Lee	*Interconnect*
Jin-Hyoung Lee	*Account Management*
Shin Kook Lee	*Interconnect*
Chan Lim	*Front End Processes*
Jae Eun Lim	*Front End Processes*
Ihn-Hong Min	*MM&P*
Sang Kyun Park	*Interconnect*
IBM	
Ricky Amos	*Front End Processes*
Stanislav Bajuk	*Lithography*
Allen Bates	*Lithography*
Robert Bates	*Lithography*
Leon Bentson	*MM&P*
Wallace Carpenter	*Lithography*
Maria Coleman	*ATDF*
Peter Dahlgren	*ESH*
Alain Deleporte	*Lithography*
Denis Fandel	*MM&P*
Michael Freiler	*Interconnect*
Glenn Gale	*Front End Processes*
Michael Jackson	*Front End Processes*
Paul Lefevre	*Interconnect*
Christopher Long	*ESH*
Walter Mlynko	*Interconnect*
John Pace	*MM&P*
Infineon	
Ann Ball	*Account Management*
Steven Bassett	*Lithography*
Renate Bergmann	*Front End Processes*
Klaus Eisner	*Lithography*
Eric Graetz	*Front End Processes*
Gerhard Gross	*Lithography*
Stefan Hien	*Lithography*
Manuela Huber	*ESH*
Stefan Lang	*MM&P*
Karsten Mosig	*Interconnect*
Hans-Erich Raske	*Lithography*
Tina Trimble	*Account Management*
Dennis Villar	*MM&P*
Juergen Woehl	*ATDF*
Intel	
Avinash Agarwal	*Front End Processes*
Chi Au	*MM&P*
Julie Calloway	*ATDF*
Wesley Calloway	*ATDF*
Jerry Cullins	*Lithography*
Tim Decker	*ATDF*
Ted Doros	*ATDF*
Jody Duke	*ATDF*
Noel Durrant	*Supplier Relations & Corporate Services*
Brian Fetzer	*ATDF*
Alfonso Garcia	*MM&P*
Patrick Kofron	*Interconnect*
Jeffrey Lee	*Interconnect*
Timothy Marbeiter	*Interconnect*
Christopher McDonald	*ATDF*
Edward Muzio	*Lithography*
John Ormando	*Interconnect*
Navid Pazand	*ATDF*
Lisa A. Scotford	*Account Management*
Zhijiang Sun	*Interconnect*
Lee Tye	*Interconnect*
Neil Wester	*Lithography*
Jeffry Worsham	*ATDF* ▶



Assignees (continued)

Lucent

Edward Akers	*Supplier Relations & Corporate Services*
Melissa Brown	*MM&P*
Aaron Frank	*Interconnect*
Cesar Garza	*Lithography*
Neil Gayle	*Supplier Relations & Corporate Services*
Matthew Huber	*MM&P*
Michael Laughery	*Front End Processes*
Tony Peoples	*MM&P*
Ronald Remke	*ESH*
Frank Sepko	*ATDF*

Motorola

Willard Conley	*Lithography*
Robert Duffin	*ESH*
Leeann English	*ESH*
Robert Fox	*Interconnect*
Roger Gladhart	*MM&P*
Ronald Gordon	*Lithography*
Chung-Peng Ho	*ATDF*
Vidya Kaushik	*Front End Processes/ IMEC*
Eric Lee	*Interconnect*
Pak Leung	*Interconnect*
Martin McCallum	*Lithography*
David Omeara	*Front End Processes*
Colita Parker	*ATDF*
Sally Pawsat	*ESH*
Anne Quincy	*Account Management*
Gane Rajagopalan	*Interconnect*
Fadi Serhan	*Interconnect*
David Sing	*Front End Processes*
Timothy Stanley	*MM&P*
Edward Strickland	*Front End Processes*
Jeffrey Wetzel	*Interconnect*
Arnette Williams	*ATDF*
Paul Winebarger	*Interconnect*

National Labs

Gary Bell	*Interconnect*
Walter Gardner	*ESH*
Abbie Warrick	*ESH*

Philips

Rod Augur	*Interconnect*
Henricus Cox	*Interconnect*
Ashwin Ghatalia	*Account Management*
Thieu Jacobs	*Interconnect*
Gene McKennie	*MM&P*
Robert Morton	*Lithography*
Klaus Pfeifer	*Interconnect*
Steven Smith	*Interconnect*

STMicroelectronics

Gilles Amblard	*Lithography*
Gordon Bease	*MM&P*
Giovanni Bianucci	*Lithography*
Olivier Louveau	*ATDF*
Paul Patruno	*Account Management*
Benoit Reynier	*MM&P*
Carmelo Romeo	*Lithography*

Texas Instruments

Ed Mickler	*Interconnect*
Byron Ahlburn	*Interconnect*
Marylyn Bennett	*ESH*
Kenneth Brennan	*Interconnect*
George Brown	*Front End Processes*
Peijun Chen	*Front End Processes*
Rinn Cleavelin	*Office of the Chief Executive*
Michael Daniels	*Interconnect*
Douglas Fischer	*Lithography*
Devarajan Ganesan	*Interconnect*
Robert Havemann	*Interconnect*
Qing-Tang Jiang	*Interconnect*
Changming Jin	*Interconnect*
Ross Jones	*ESH*
Won Kim	*Lithography*
Edward Mickler	*Interconnect*
Coleen Miller	*ESH*
Robert Murto	*Front End Processes*
Stephen Strausser	*Interconnect*
Victor Watt	*Front End Processes*
Robin Worley	*Front End Processes*
Mike Zimmermann	*Account Management*

TSMC

Chih-Cheng Lin	*Lithography*
Steven Lin	*Front End Processes*
Su-Horng Lin	*Interconnect*
Ming-Huei Lui	*Interconnect*
Dah-Chung Owe-Yang	*ATDF*
Ming-Hsing Tsai	*Interconnect*
Wei-Kun Yeh	*Account Management* ■

key contacts

Key Contacts

Company	Assignee Coordinator	Tech Transfer Manager	Account Executive	Senior Assignee
Agere (formerly Lucent)	Dale Ibbotson 407/371-6060 ordei@micro.lucent.com	Don Lindholm 512/356-3790 don.lindholm@sematech.org	Don Lindholm 512/356-3790 don.lindholm@sematech.org	Ron Remke 512/356-7090 ron.remke@sematech.org
AMD	David Bennett 512/602-5930 david.bennett@amd.com	Dan Gockel 512/602-4649 dan.gockel@amd.com	Clete Deller 512/356-3178 clete.deller@sematech.org	Marlin Shopbell 512/356-7493 marlin.shopbell@sematech.org
Conexant	Jerry Brandewie 512/356-3449 jerry.brandewie@sematech.org	Jerry Brandewie 512/356-3449 jerry.brandewie@sematech.org	Jerry Brandewie 512/356-3449 jerry.brandewie@sematech.org	Volker Blaschke 512/356-3964 volker.blaschke@sematech.org
Hewlett-Packard	Clete Deller 512/356-3178 clete.deller@sematech.org	Clete Deller 512/356-3178 clete.deller@sematech.org	Clete Deller 512/356-3178 clete.deller@sematech.org	Ken Vandehey 512/356-3418 ken.vandehey@sematech.org
Hynix (formerly Hyundai)	C.S. Park 011-82-336-30-4530 cspark@sr.hei.co.kr	Jin-Hyoung Lee 512/356-3023 jin-hyoung.lee@sematech.org	Jin-Hyoung Lee 512/356-3023 jin-hyoung.lee@sematech.org	Shin Kook Lee 512/356-3550 shinkook.lee@sematech.org
IBM	Denny Johnson 802/769-8523 dmjohnso@us.ibm.com	Denny Johnson 802/769-8523 dmjohnso@us.ibm.com	M.J. (Spike) Myers 512/356-3183 m.j.myers@sematech.org	Mike Jackson 512/356-6794 mike.jackson@sematech.org
Infineon	Susanne Zang 011-49-89-234-26733 susanne.zang@infineon.com	Tina Trimble 512/356-7861 tina.trimble@sematech.org	Tina Trimble 512/356-7861 tina.trimble@sematech.org	Juergen Woehl 512/356-7147 juergen.woehl@sematech.org
Intel	Michael J. Ryan 916/356-2207 michael.j.ryan@intel.com	Michael J. Ryan 916/356-2207 michael.j.ryan@intel.com	Michael J. Ryan 916/356-2207 michael.j.ryan@intel.com	Giang Dao 512/356-7470 giang.dao@sematech.org
Motorola	Laurie Beu 512/933-5457 rwbh30@email.sps.mot.com	Laurie Beu 512/933-5457 rwbh30@email.sps.mot.com	Bill Donaldson 512/356-3912 bill.donaldson@sematech.org	Navjot Chhabra 512/356-3752 navjot.chhabra@sematech.org
Philips	Maurits Wilts 011-31-40-27-22657 maurits.wilts@philips.com	Aubin Wilkens +31-24-353-2861 aubin.wilkens@philips.com	Ashwin Ghatalia 512/356-7165 ashwin.ghatalia@sematech.org	Klaus Pfeifer 512/356-7061 klaus.pfeifer@sematech.org
STMicroelectronics	Thierry Denjean 011-33-476-926013 thierry.denjean@st.com	Paul Patruno 512/356-7679 paul.patruno@sematech.org	Paul Patruno 512/356-7679 paul.patruno@sematech.org	Paul Patruno 512/356-7679 paul.patruno@sematech.org
Texas Instruments	Mike Zimmermann 512/356-7585 mike.zimmermann@sematech.org	Mike Zimmermann 512/356-7585 mike.zimmermann@sematech.org	Mike Zimmermann 512/356-7585 mike.zimmermann@sematech.org	Coleen Miller 512/356-7430 coleen.miller@sematech.org
TSMC	Mong-Song Liang 011-886-3-578-1688 msliang@tsmc.com.tw	Kuei-Wu Huang 512/356-7137 kuei-wu.huang@sematech.org	Kuei-Wu Huang 512/356-7137 kuei-wu.huang@sematech.org	Kuei-Wu Huang 512/356-7137 kuei-wu.huang@sematech.org ■

For assignee information, contact Sean Murphy (512/356-3411; sean.murphy@sematech.org) or Mary Griffin (512/356-3448; mary.griffin@sematech.org).

Printed on recycled paper ♻

2706 Montopolis Drive
Austin, Texas 78741
(512) 356-3500
www.sematech.org

Acknowledgements:
Design: Grafico.Design
Printing: Copy Craft Printers, Inc.
Photography: Kevin Vandivier