Integrated
Circuit
Systems, Inc.

Digitally Controlled Audio Mixer

Description

The **ICS2101** is a CMOS digitally controlled multi-channel line-level stereo audio mixer for use in multimedia applications. High performance attenuators provide precision gain control in -0.5dB increments. The ten input channels may be used as mono inputs, pairs of stereo inputs, or any combination of mono and stereo inputs appropriate for the application. Stereo balance and mono panning functions are fully supported. The **ICS2101** is compatible with the ISA industry standard bus.

Features

- Five stereo input pairs
- One stereo output pair
- Precision gain control in -0.5dB steps
- Separate attenuation and balance control for each input pair
- Mono input mode with panning capability
- Master attenuation and balance control for output
- Low noise, low distortion
- ISA compatible
- 28-pin DIP or SOIC package

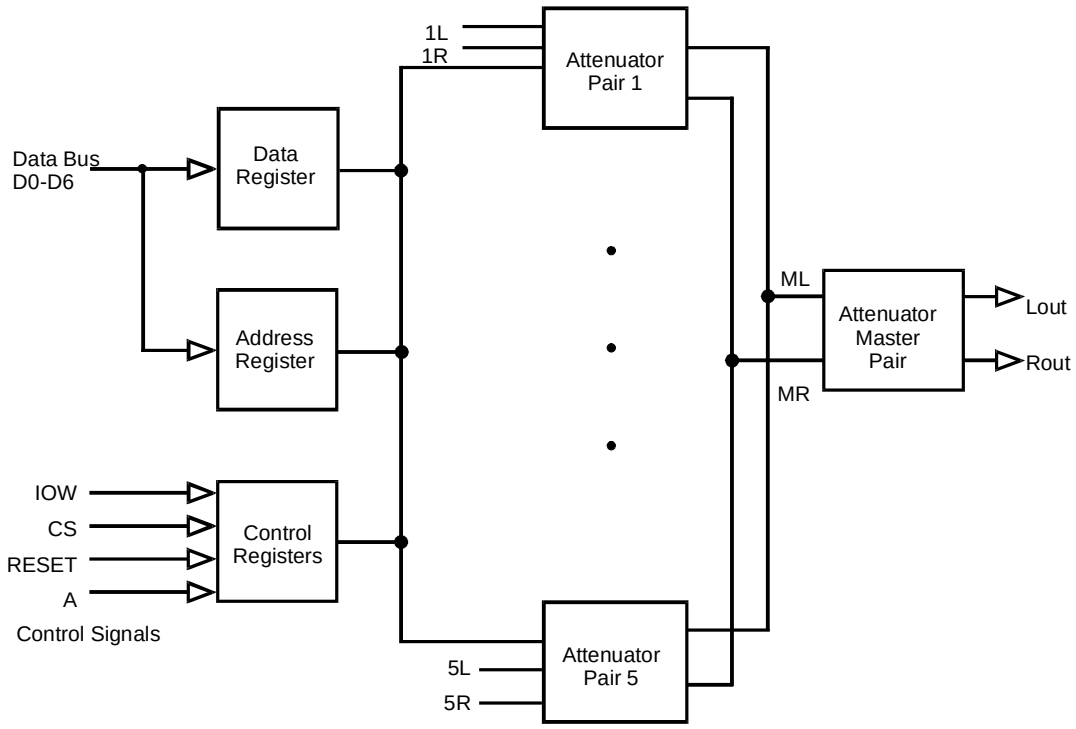
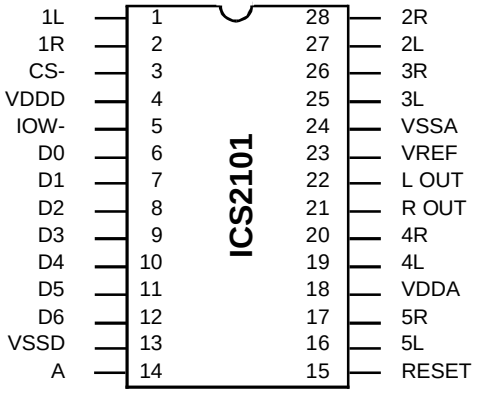


Figure 1 - Block Diagram



28-Pin DIP
28-Pin SOP

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 2, 16, 17, 19, 20, 25, 26, 27, 28	1L-5L, IR-5R	AI	Audio inputs (left and right) for attenuators 1 through 5. An external coupling capacitor should be connected to each input.
3	CS-	I	Chip select, active low.
5	IOW-	I	Input/output write, active low. Data is latched on the rising edge.
6, 7, 8, 9, 10, 11, 12	D0-D6	I	Data bus, active high.
14	A	I	Address/data select. Low input selects the data register, high input selects the address register.
15	RESET	I	Resets all registers to OOH, active high.
21, 22	Rout, Lout	AO	Line level audio outputs.
23	V_{REF}	P	Reference voltage of $0.44V_{DDA}$. A 1000 pf capacitor should be connected between V_{DDA} and V_{SSA}.
4	V_{DDD}	P	Digital power.
18	V_{DDA}	P	Analog power.
13	V_{SSD}	P	Digital ground.
24	V_{SSA}	P	Analog ground.

I=Input; O=Output; P=Power; A=Analog

Absolute Maximum Ratings

Storage Temperature. . . . . -65°C to 150°C
Voltage on any pin with
respect to ground . . . . . -0.3V to V_{DDD}+0.3V
Maximum V_{DDD}. 7V
Power Dissipation. 1W

Standard Test Conditions

Operating Temperature Range . . 0°C to 70°C
Power Supply Voltage . . . . . 4.75 to 5.25 Volts

DC Characteristics

V_{DDD} = 5V ± 5%, V_{SSD} = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{IH}	Logical 1 Input Voltage	2.4		V_{DDD}	V	
V_{IL}	Logical 0 Input Voltage	0		0.8	V	
I_{IL}	Input Leakage Current	-1		1	uA	$0 < V_{IN} < V_{DDD}$
I_{OH}	Output Source Current	-100			mA	$V_{OUT} = V_{REF}$ + 1V Master attenuator off
I_{OL}	Output Sink Current			100	mA	$V_{OUT} = V_{REF}$ - 1V Master attenuator off
V_{REF}	Internal Reference V		.44 V_{DDD}		V	
I_{ADD}	Analog Supply Current		7	10	mA	
I_{DDD}	Digital Supply Current		10	100	µA	

AC Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
ANALOG						
V_{AI}	Analog Input Voltage			3	Vp-p	AC coupled
A_F	Analog Frequency Range	20		20,000	Hz	
R_{IN}	Attenuator Input Resistance	20	32		k ohm	Gain = 0dB
T_{HD}	Total Harmonic Distortion		0.2		%	2Vp-p, 1 kHz, Gain = 0dB
S_{NR}	Signal to Noise Ratio		86		dB	Gain = 0dB BW = 20 to 20 kHz
R_{MONO}	Mono Switch Resistance	100	200	400	ohms	
N_{CR}	Crosstalk - L/R Channel		78		dB	1 kHz, 2 V_{P-P} Gain = 0db
ΔG	Analog Output Step		0.5		dB	Atten. value 127 through 16
DIGITAL						
T_{RESET}	Reset Pulse Width	200			ns	
T_{IOWL}	IOW Pulse Width Low	80			ns	
T_{IOWH}	IOW Pulse Width High	120			ns	
T_{CSS}	Chip Select Setup Time	25			ns	
T_{CSH}	Chip Select Hold Time	25			ns	
T_{DS}	Data Setup Time	25			ns	
T_{DH}	Data Hold Time	25			ns	

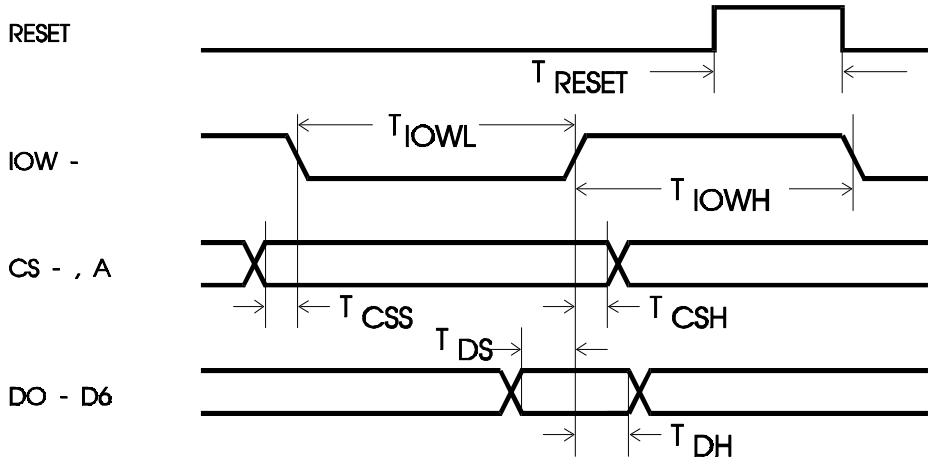


Figure 2 - Input Bus Timing

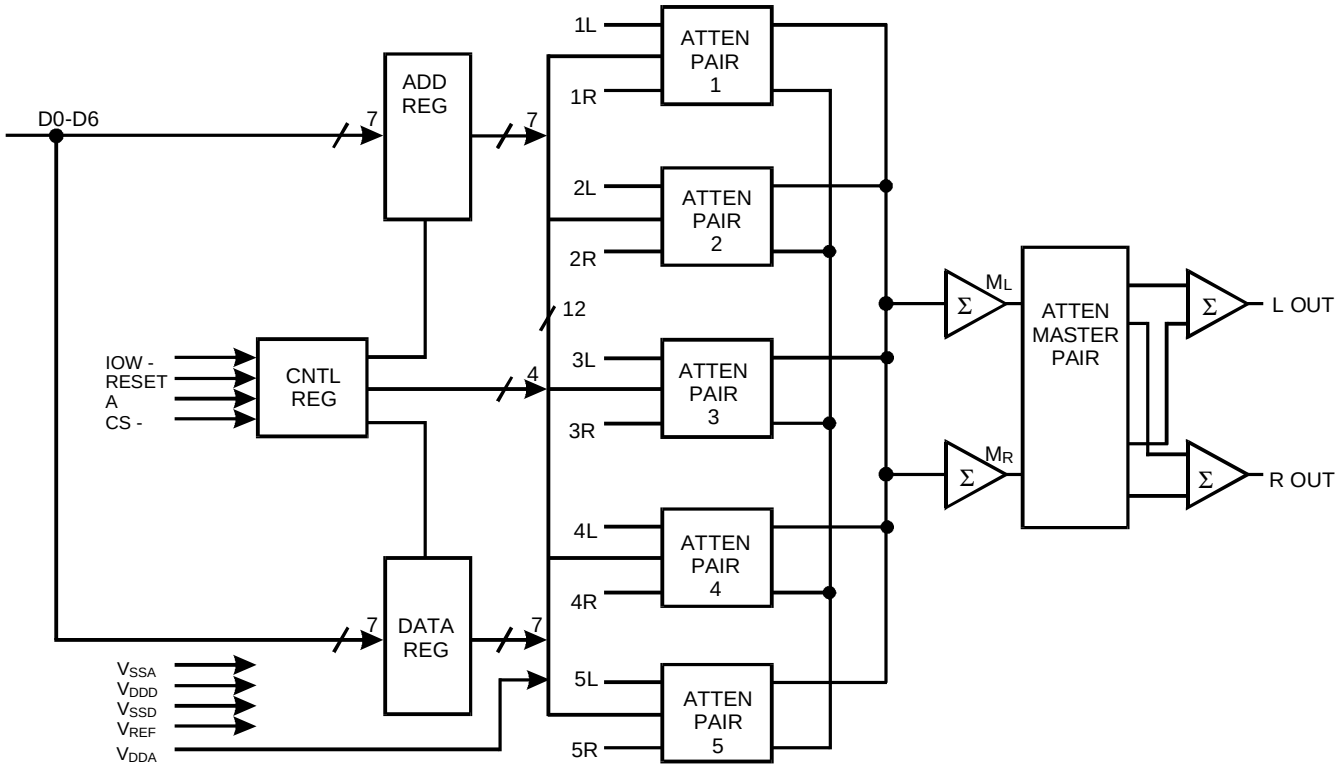
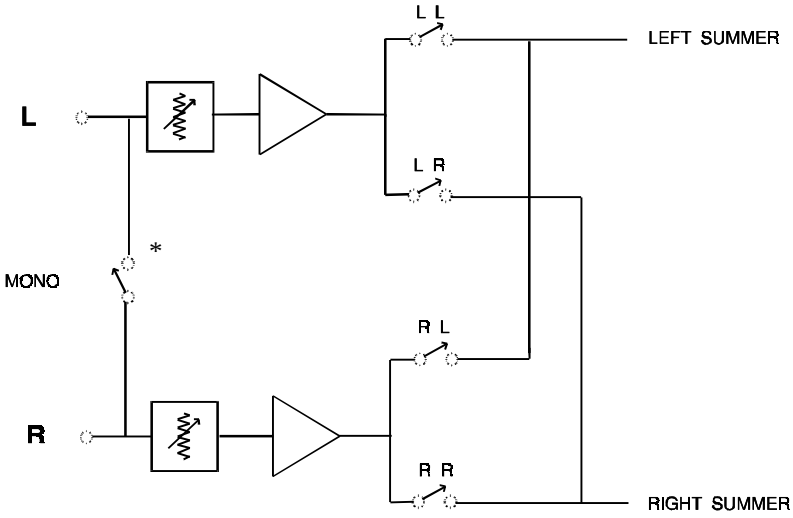


Figure 3 - Block Diagram



* The master attenuator pair does not have a mono switch; the connection between the left and right inputs is open.

Figure 4 - Attenuator Pair Detail

Timing Diagram

Programming

The **ICS2101** mixer provides two write-only registers (address and data) the host processor can use. Typically the host writes a value to the address register, selecting the appropriate data register for the subsequent data-write operations. For applications such as gradually fading one attenuator, the address register can be written to once at the beginning of the operation. A new data value is needed only when a different attenuator is selected.

Address Register

The address register is used to point to internal registers (attenuator and control).

Data Definition

D6	D5	D4	D3	D2	D1	D0
X	-	-	-	-	-	-
	Attenuator Selection			Control Selection		

Attenuator and Control Register Selection

D6	D5	D4	D3	D2	D1	D0	Attenuator and Control Register Definition
X	X	X	X	0	0	0	Control Left
X	X	X	X	0	0	1	Control Right
X	X	X	X	0	1	0	Attenuator Left
X	X	X	X	0	1	1	Attenuator Right
X	X	X	X	1	0	X	Pan/Balance
X	0	0	0	X	X	X	Pair 1
X	0	0	1	X	X	X	Pair 2
X	0	1	0	X	X	X	Pair 3
X	0	1	1	X	X	X	Pair 4
X	1	0	0	X	X	X	Pair 5
X	1	0	1	X	X	X	Master

Attenuation Register

Each attenuator is controlled by a 7-bit value written to the control register. The values of 127 through 16 will increase the attenuation linearly in one-half decibel (dB) increments. Values of 15 through 0 will cause the attenuation to increase at an increasing rate, with a value of 00H corresponding to maximum attenuation. The channel is off when the control register value is 00H and at maximum volume (completely on) with a value of 7FH.

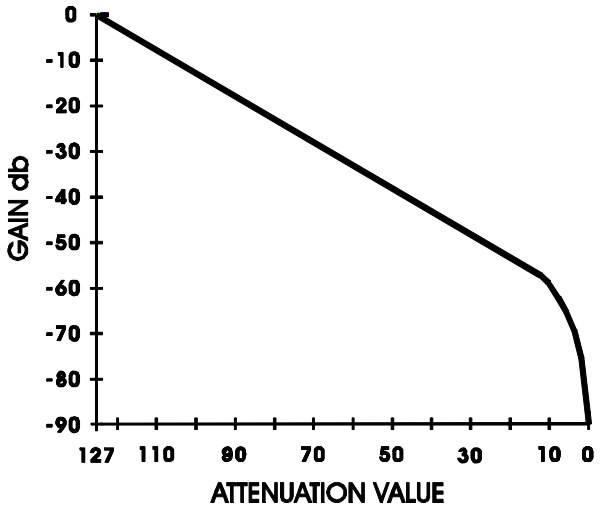


Figure 5 - Gain vs. Control Value

Modes of Operation

Each attenuator pair may operate in one of three modes:

- Normal mode
- Stereo mode
- Balance/Pan mode

Normal Mode

Normal mode is used for applications with mono inputs. In this mode, both internal attenuator (left and right) and control registers (left and right) are utilized. Each may be controlled separately.

Stereo Mode

The operation of the attenuator pair in stereo mode is controlled by the left control register. The data written to the left control register is also written to the right control register; therefore, application software need not write to the right control or right attenuation register while operating in this mode. The gain of both channels will be identical in stereo mode. The master attenuator pair does not have a mono switch and cannot be operated in any mode requiring the mono switch to be in the closed (or on) position.

Balance/Pan Mode

The operation of the attenuator pair in balance/pan mode is controlled by the left control register. The data written to the left control register is also written to the right control register; therefore, need not write to the right control or right attenuation register while operating in this mode. The balance/pan register controls the gain of the attenuator pair by regulating the balance and the pan position of the output signals. The master attenuator pair does not have a mono switch and cannot be operated in any mode requiring the mono switch to be in the closed (or on) position. The master attenuator pair cannot be used in pan mode.

In the pan/balance mode, two separate registers are used to control the attenuator pair. The attenuation value directed to the left attenuator register is modified by the contents of the pan/balance register, and the appropriate values are then written to the left and right attenuator registers. When the pan/balance register of a channel is modified, the data value has no effect on the attenuator settings until the next value is written to the left attenuator register.

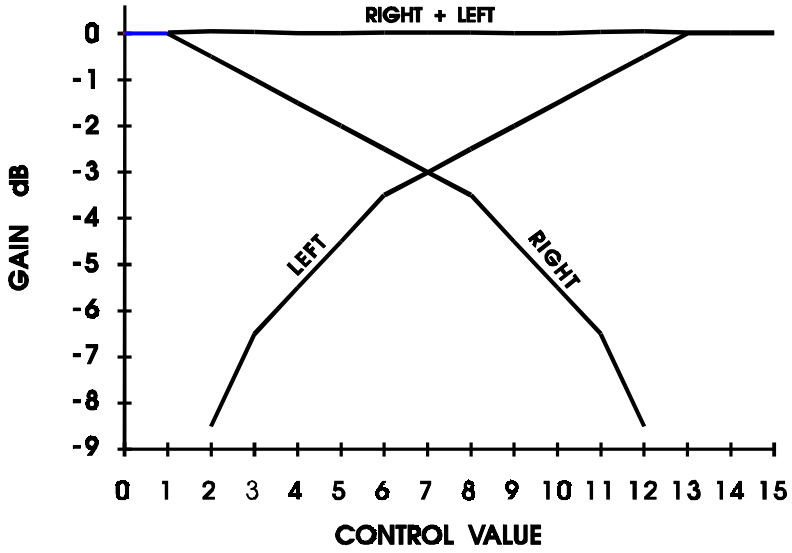


Figure 6 - Gain vs. Control Value

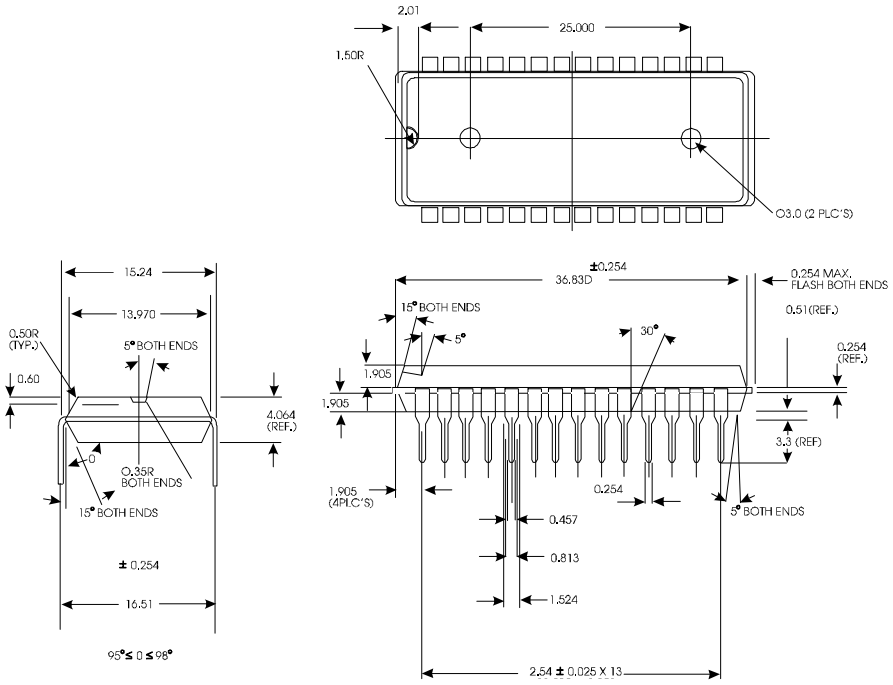
Modes of Operation - Data Values and Switch Settings

Right Control Register

D6	D5	D4	D3	D2	D1	D0	LL	LR	RL	RR	Mono	Mode of Operation
X	X	X	0	0	0	0	X	X	Off	Off	Off	Normal
X	X	X	0	0	0	1	X	X	On	Off	Off	Normal
X	X	X	0	0	1	0	X	X	Off	On	Off	Normal
X	X	X	0	0	1	1	X	X	On	On	Off	Normal

Left Control Register

D6	D5	D4	D3	D2	D1	D0	LL	LR	RL	RR	Mono	Mode of Operation
X	X	X	0	0	0	0	Off	Off	X	X	Off	Normal
X	X	X	0	0	0	1	On	Off	X	X	Off	Normal
X	X	X	0	0	1	0	Off	On	X	X	Off	Normal
X	X	X	0	0	1	1	On	On	X	X	Off	Normal
X	X	X	0	1	0	0	On	Off	Off	On	Off	Stereo - Normal
X	X	X	0	1	0	1	Off	On	On	Off	Off	Stereo - Reversed Channels
X	X	X	0	1	1	0	On	Off	Off	On	On	Mono
X	X	X	0	1	1	1	Off	On	On	Off	On	Mono (Reserved)
X	X	X	1	0	0	0	On	Off	Off	On	Off	Balance - Normal
X	X	X	1	0	0	1	Off	On	On	Off	Off	Balance - Reversed Channels
X	X	X	1	0	1	0	On	Off	Off	On	On	Pan - Normal
X	X	X	1	0	1	1	Off	On	On	Off	On	Pan - Reversed



28-Pin DIP Package

Ordering Information

ICS2101N

Example:

ICS XXXX M

Package Type
N=DIP (Plastic)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device