VT82C597
VT82C597AT

Apollo VP3

Single-Chip North Bridge
for Pentium / Socket-7
with AGP and PCI
plus Advanced ECC Memory Controller
supporting DDR SDRAM-II,
SDRAM, EDO, and FPG

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REVISION HISTORY

Document Release	Date	Revision	Initials
0.1	3/28/97	Original release (VIA internal review only)	DH
0.2	4/1/97	Changed memory technologies supported to FP,EDO,SDRAM,SDRAM-II Fixed Introduction and Feature bullets per engineering review Rearranged registers to clarify that registers 50-8F are device 0 Added pin descriptions for DS[3:0], GGNT#, and clocks Fixed miscellaneous register bit descriptions per engineering review	DH
0.3	4/29/97	Added 456-pin BGA Mechanical Specification drawing Rearranged pin groupings and changed pinouts per PCB floorplanning Updated register definitions to reflect internal spec Rev 0.5 (4/15/97)	DH
0.4	5/14/97	Updated pinouts to reflect final pinout after chip layout / pad placement Updated Feature Bullets and Overview to reflect final chip design Updated pin descriptions per engineering input and final chip design Updated register descriptions per engineering input and final chip design	DH
0.5	5/15/97	Updated pinouts (MD, MPD, & CAS pin swaps). Per 5/15/97 engg spec Added pin descriptions for GVREF, MVREF, AVCC, AGND	DH
0.6	5/21/97	Changed package from 456-pin to 472-pin BGA - updated mechanical spec Updated pinouts: added 16 grounds in package center Updated pinouts: changed 4 GND pins to CVCC (supply for internal logic) Updated pinouts: changed 2 HVCC pins to MVCC Updated pin descriptions for clock pins	DH
0.7	6/16/97	Removed “NDA Required” watermark (product announced at Computex) Moved ground balls from M9-M10 to N9-N10 (fixed pinouts and mechanical) Added central-DQ support (feature bullets and register bits) Fixed typos (block diagram BGA ball count, and alpha pin list J18)	DH
0.8	9/22/97	Fixed feature bullets in AGP and memory controller sections Fixed Pinouts & Pin Definitions: 597 pinout error: CAS1 swapped with CAS2; CAS5 swapped with CAS6 Added 82C597AT pinouts Updated pin definitions and signal names (SBS#, ADS0-1#) Removed COE2# and CCS2# functionality from TA8-9 (not implemented) Added MWEA# and MWEB# function on SWEA# and SWEB# Added AGP PCB layout notes Changed AGP clock (GCLK) to grounded input (generated internally) Fixed Register Descriptions: Added Chip Revision info to Device 0 Rx08 Fixed typos in Device 0 Rx10, Rx58, and RxAC Updated bit definitions in Device 0 Rx64, 68, 6C, 70, 71, 76, 80, 88, and AC Added Device 0 Rx6B DRAM Arbitration Control Added Device 0 Rx74 PCI Master Control 2 Added Device 0 Rx77 Chip Test, Rx7E DLL/DLL4 Test, Rx7F DLL4 Test Added Device 1 Rx3E PCI-to-PCI Bridge Control Updated bit definitions in Device 1 Rx40 and 42 Added Electrical Specifications & Timing Diagrams	DH
1.0	10/3/97	Timing Diagrams redrawn to reduce final PDF file size Timing Specification AC Timing numbers rounded to one decimal place Timing Specification AC Timing Table 8 numbers updated Changed name of ADS[1-0]# to GDS[1-0]# reduce confusion with ADS# Added new VIA logos and removed “Preliminary” from document revision	DH

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Single-Chip North Bridge
for Pentium / Socket-7
with AGP and PCI
plus Advanced ECC Memory Controller
supporting DDR SDRAM-II,
SDRAM, EDO, and FPG

- **PCI/ISA Green PC Ready**
  - Supports separately powered 3.3V (5V tolerant) interfaces to system memory, AGP, and PCI bus
  - Supports 3.3V and sub-3.3V interface to CPU
  - PC-97 compatible using VT82C586B South Bridge with ACPI Power Management
- **High Integration**
  - Single chip implementation for 64-bit Socket-7-CPU, 64-bit system memory, 32-bit PCI and 32-bit AGP interfaces
  - **Apollo VP3** Chipset: **VT82C597 or VT82C597AT** system controller and **VT82C586B** PCI to ISA bridge
  - Chipset includes UltraDMA-33 EIDE, USB, and Keyboard / PS2-Mouse Interfaces plus RTC / CMOS on chip
- **Flexible CPU Interface**
  - Supports 64-bit Pentium™, AMD 5_K86™ , AMD 6_K86™ and Cyrix 6_X86™ CPUs
  - CPU external bus speed up to 66 MHz (internal 233MHz and above)
  - Supports CPU internal write-back cache
  - System management interrupt, memory remap and STPCLK mechanism
  - Cyrix 6_X86 linear burst support
  - CPU NA# / Address pipeline capability
  - 4 cache lines of CPU/cache-to-DRAM post-write buffers
  - 4 quadwords of CPU/cache-to-DRAM read-prefetch buffers
- **Advanced Cache Controller**
  - Direct map write back or write through secondary cache
  - Pipelined burst synchronous SRAM (PBSRAM) cache support (with global write enable feature)
  - Flexible cache size: 0K / 256K / 512K / 1M / 2MB
  - 32 byte line size to match the primary cache
  - Integrated 10-bit tag comparator
  - 3-1-1-1 read/write timing for PBSRAM access at 66 MHz
  - 3-1-1-1-1-1-1-1 back to back read timing for PBSRAM access at 66 MHz
  - Sustained 3 cycle write access for PBSRAM access or CPU to DRAM and PCI bus post write buffers at 66 MHz
  - Data streaming for simultaneous primary and secondary cache line fill
  - System and video BIOS cacheable and write-protect
  - Programmable cacheable region and cache timing

- **AGP Controller**
  - AGP v1.0 compliant
  - Supports SideBand Addressing (SBA) mode (non-multiplexed address / data)
  - Supports 133MHz 2X mode for AD and SBA signalling
  - Pipelined split-transaction long-burst transfers up to 533 MB/sec
  - Eight level read request queue
  - Four level posted-write request queue
  - Thirty-two level (quadwords) read data FIFO (128 bytes)
  - Sixteen level (quadwords) write data FIFO (64 bytes)
  - Intelligent request reordering for maximum AGP bus utilization
  - Supports Flush/Fence commands
- **GART**
  - One level TLB structure
  - Sixteen entry fully associative page table
  - LRU replacement scheme
  - Independent GART lookup control for host / AGP / PCI master accesses
- **Intelligent PCI Bus Controller**
  - PCI buses are synchronous to host CPU bus
  - 33 MHz operation on the primary PCI bus
  - 66 MHz PCI operation on the AGP bus
  - PCI-to-PCI bridge configuration on the 66MHz PCI bus
  - Separate data buffers for the two PCI buses
  - Peer concurrency
  - Concurrent multiple PCI master transactions; i.e., allow PCI masters from both PCI buses active at the same time
  - Allows PCI master access while ISA master/DMA is active
  - PCI master snoop ahead and snoop filtering
  - Five levels (double-words) of CPU to PCI posted write buffers
  - Byte merging in the write buffers to reduce the number of PCI cycles and to create further PCI bursting possibilities
  - Zero wait state PCI master and slave burst transfer rate
  - PCI to system memory data streaming up to 132Mbyte/sec
  - Enhanced PCI command optimization (MRL, MRM, MWI, etc.)
  - Forty-eight levels (double-words) of post write buffers from PCI masters to DRAM
  - Sixteen levels (double-words) of prefetch buffers from DRAM for access by PCI masters
  - Supports L1/L2 write-back forward to PCI master read to minimize PCI read latency
  - Supports L1/L2 write-back merged with PCI master post-write to minimize DRAM utilization
  - Transaction timer for fair arbitration between PCI masters (granularity of two PCI clocks)
  - Symmetric arbitration between Host/PCI bus for optimized system performance
  - Complete steerable PCI interrupts
  - PCI-2.1 compliant, 32 bit 3.3V PCI interface with 5V tolerant inputs

- **Advanced High-Performance DRAM Controller**
  - 66MHz DRAM interface
  - Concurrent CPU and AGP access
  - FP, EDO, SDRAM, and SDRAM-II
  - 66MHz DDR (Double Data Rate) supported for SDRAM-II (supports central and edge DQ, bidirectional DS, and optional SDR write)
  - Different DRAM types may be used in mixed combinations
  - Different DRAM timing for each bank
  - Mixed 1M / 2M / 4M / 8M / 16MxN DRAMs
  - 6 banks up to 1GB DRAMs
  - Flexible row and column addresses
  - 64-bit data width only
  - 3.3V DRAM interface with 5V-tolerant inputs
  - Optional bank-by-bank ECC (single-bit error correction and multi-bit error detection) or EC (error checking only) for DRAM integrity
  - Two-bank interleaving for 16Mbit SDRAM support
  - Two-bank and four bank interleaving for 64Mbit SDRAM support (14 MA lines)
  - Supports maximum 8-bank interleave (i.e., 8 pages open simultaneously); banks are allocated based on LRU
  - Seamless DRAM command scheduling for maximum DRAM bus utilization (e.g., precharge other banks while accessing the current bank)
  - Four cache lines (16 quadwords) of CPU/cache to DRAM write buffers
  - Concurrent DRAM writeback
  - Read around write capability for non-stalled CPU read
  - Burst read and write operation
  - 5-2-2-2 on page, 8-2-2-2 start page and 11-2-2-2 off page timing for EDO DRAMs at 66 MHz
  - 6-1-1-1 on page, 8-1-1-1 start page and 10-1-1-1 off page for SDRAMs at 66 MHz
  - 5-2-2-2-3-2-2-2 back-to-back accesses for EDO DRAM at 66 MHz
  - 6-1-1-1-3-1-1-1 back-to-back accesses for SDRAM at 66 MHz
  - BIOS shadow at 16KB increment
  - Decoupled and burst DRAM refresh with staggered RAS timing
  - Programmable refresh rate, CAS-before-RAS refresh and refresh on populated banks only
- **Built-in NAND-tree pin scan test capability**
- **3.3V, 0.5um, high speed / low power CMOS process**
- **472 pin BGA Package**
- **Alternate pinouts available to optimally accommodate different PCB form factors**
  - VT82C597 for ATX and NLX
  - VT82C597AT for Baby AT and ATX

OVERVIEW

The ***Apollo-VP3*** is a high performance, cost-effective and energy efficient chip set for the implementation of AGP / PCI / ISA desktop and notebook personal computer systems based on 64-bit Socket-7 (Intel Pentium and Pentium MMX; AMD K5 / 5_K86 and K6 / 6_K86; and Cyrix / IBM 6_x86 / M2) super-scalar processors.

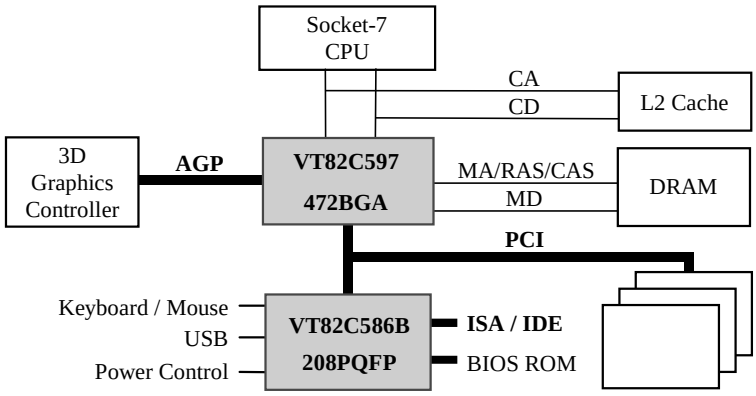


Figure 1. Apollo VP3 System Block Diagram

The Apollo-VP3 chip set consists of the VT82C597 system controller (472 pin BGA) and the VT82C586B PCI to ISA bridge (208 pin PQFP). The VT82C597 system controller provides superior performance between the CPU, optional synchronous cache, DRAM, AGP bus, and PCI bus with pipelined, burst, and concurrent operation. For pipelined burst synchronous SRAMs, 3-1-1-1-1-1-1-1 timing can be achieved for both read and write transactions at 66 MHz. Four cache lines (16 quadwords) of CPU/cache to DRAM write buffers with concurrent write-back capability are included on chip to speed up cache read and write miss cycles.

The VT82C597 supports six banks of DRAMs up to 1GB. The DRAM controller supports standard Fast Page Mode (FPM) DRAM, EDO-DRAM, Synchronous DRAM (SDRAM), and SDRAM-II with Double Data Rate (DDR) in a flexible mix / match manner. The Synchronous DRAM interface allows zero wait state bursting between the DRAM and the data buffers at 66Mhz. The six banks of DRAM can be composed of an arbitrary mixture of 1M / 2M / 4M / 8M / 16MxN DRAMs. The DRAM controller also supports optional ECC (single-bit error correction and multi-bit detection) or EC (error checking) capability separately selectable on a bank-by-bank basis.

The VT82C597 also supports full AGP v1.0 capability for maximum bus utilization including 2x mode transfers, SBA (SideBand Addressing), Flush/Fence commands, and pipelined grants. An eight level request queue plus a four level post-write request queue with thirty-two and sixteen quadwords of read and write data FIFO's respectively are included for deep pipelined and split AGP transactions. A single-level GART TLB with 16 full associative entries and flexible CPU/AGP/PCI remapping control is also provided for operation under protected mode operating environments.

The VT82C597 supports two 32-bit 3.3 / 5V system buses (one AGP and one PCI) with 64-bit to 32-bit data conversion. The 82C597 also contains a built-in bus-to-bus bridge to allow simultaneous concurrent operations on each bus. Five levels (doublewords) of post write buffers are included to allow for concurrent CPU and PCI operation. Consecutive CPU addresses are converted into burst PCI cycles with byte merging capability for optimal CPU to PCI throughput. For PCI master operation, forty-eight levels (doublewords) of post write buffers and sixteen levels (doublewords) of prefetch buffers are included for concurrent PCI bus and DRAM/cache accesses. The chipset also supports enhanced PCI bus commands such as Memory-Read-Line, Memory-Read-Multiple and Memory-Write-Invalid commands to minimize snoop overhead. In addition, the chipset supports advanced features such as snoop ahead, snoop filtering, L1 write-back forward to PCI master and L1 write-back merged with PCI post write buffers to minimize PCI master read latency and DRAM utilization. The VT82C586B PCI to ISA bridge supports four levels (doublewords) of line buffers, type F DMA transfers and delay transaction to allow efficient PCI bus utilization and (PCI-2.1 compliant). The VT82C586B also includes an integrated keyboard controller with PS2 mouse support, integrated DS12885 style real time clock with extended 256 byte CMOS RAM, integrated master mode enhanced IDE controller with full scatter and gather capability and extension to UltraDMA-33 / ATA-33 for 33MB/sec transfer rate, integrated USB interface with root hub and two function ports with built-in physical layer transceivers, Distributed DMA support, and OnNow / ACPI compliant advanced configuration and power management interface. A complete main board can be implemented with only six TTLs.

The Apollo VP3 chipset is ideal for high performance, high quality, high energy efficient and high integration desktop and notebook AGP / PCI / ISA computer systems.

PINOUTS

Figure 2. VT82C597 Ball Diagram (Top View)

Key	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	MD58	MD27	MD28	MD61	MD63	GD1	GD7	GBE0#	GD11	GBE1#	GTRDY#	GD17	GD20	GD25	GD28	GD31	SBA5	SBA1	ST0	GREQ#	GPAR	STOP#	AD17	AD21	AD22	AD23
B	MD57	MD26	MD59	MD29	MD31	GD0	GD4	GDS0#	GD12	GD15	GDSEL#	GFRM#	GD19	GBE3#	GD26	GD29	SBA4	SBA3	GPIPE#	ST1	GGNT#	LOCK#	AD16	AD19	AD20	CBE3#
C	MD24	MD56	MD25	MD60	MD62	GD5	GD2	GD6	GD9	GD13	GSTOP	GIRDY	GD18	GD22	GD24	GD30	SBA7	SBS#	GRBF#	GSERR#	-res-	SERR#	CBE2#	AD18	AD24	AD25
D	MD22	MD54	MD23	MD55	MD30	GD8	GD3	GND	GD10	GD14	GBE2#	GD21	GD23	GDS1#	GD27	SBA6	SBA2	SBA0	PCLK	PAR	ST2	AD0	AD1	AD27	AD26	AD28
E	MD52	MD21	MD53	DS3#	CVCC	GND	GND	GCLK	GVCC	GVCC	GVCC	GD16	GVRE	GND	GND	GND	GVCC	GVCC	GVCC	-res-	5VREF	GND	AD2	AD29	AD30	AD31
F	MD19	MD51	MD20	DS1#	AVCC	F6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	F21	CVCC	AD3	REQ0#	GNT0#	REQ1#
G	MD49	MD18	MD50	MD17	MVCC	G	Data		Total = 472 Pins				AGP Pins								G	AD5	AD4	GNT1#	REQ2#	GNT2#
H	SWEC#	MD16	MD48	MPD7	MVCC	H			9	10	11	12	13	14	15	16	17	18		PCI Pins	H	AD6	AD7	REQ3#	GNT3#	AD14
J	CAS7#	SWEA#	SWEB#	MPD3	MVCC	J		J	GND					GND				GND	J		J	PVCC	AD8	AD15	CBE1#	DSEL#
K	CAS1#	CAS5#	CAS3#	MPD2	AGND	K	Control	K		GND	11	12	13	GND	15	16	GND		K		K	PVCC	CBE0#	AD9	TRDY#	IRDY#
L	RAS3#	RAS1#	RAS0#	MPD6	GND	L		L		L	GND	GND	GND	GND	GND	GND			L		L	PVCC	AD10	AD12	FRM#	PGNT#
M	MAA1	RAS5#	RAS4#	RAS2#	GND	M	Mem Pins	M		M	GND	GND	GND	GND	GND	GND			M		M	AD11	AD13	PREQ#	RESET#	TA2
N	MA12	MA13	MAA0	MA8	HCLK	N		N	GND	GND	GND	GND	GND	GND	GND	GND			N	Cache	N	TA5	TA4	TA3	TA0	TA1
P	MA9	MA10	MA11	MA4	MVREF	P	Address	P		P	GND	GND	GND	GND	GND	GND	GND	GND	P		P	GND	TA8	TWE#	TA6	TA7
R	MA5	MA6	MA7	MAB0	MVCC	R		R		R	GND	GND	GND	GND	GND	GND			R		R	GND	BWE#	CCS1#	COE1#	TA9
T	MAB1	MA2	MA3	CAS2#	MVCC	T		T		T	GND	GND	GND	GND	GND	GND			T		T	HD1	HD0	CADV#	CADS#	GWE#
U	SRASC	SRASB#	SRASA#	DS0#	MVCC	U	Control	U		GND			GND				GND		U		U	HVCC	HD5	HD4	HD3	HD2
V	CAS0#	CAS4#	CAS6#	DS2#	MVCC	V		V	GND				GND					GND	V		V	HVCC	HD9	HD8	HD7	HD6
W	SCASC	SCASB#	SCASA#	MPD5	MPD1	W			9	10	11	12	13	14	15	16	17	18			W	HD14	HD13	HD12	HD11	HD10
Y	MD46	MD15	MD47	MPD4	GND	Y	Data	Control				Address		CPU Pins		Byte Enables				Data	Y	HD19	HD18	HD17	HD16	HD15
AA	MD13	MD45	MD14	MPD0	GND	AA6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	AA21	GND	HD23	HD22	HD21	HD20
AB	MD43	MD12	MD44	MD11	CVCC	MVCC	MVCC	5VREF	HVCC	HVCC	HA25	HA30	GND	GND	HA8	BE5#	HVCC	HVCC	HVCC	HD52	CVCC	GND	HD27	HD26	HD25	HD24
AC	MD41	MD10	MD42	MD9	MD33	MD32	MD1	BRDY#	M/IO#	HA27	HA28	HA17	HA14	HA3	HA7	BE6#	BE1#	HD61	HD57	HD53	HD48	HD44	HD31	HD30	HD29	HD28
AD	MD8	MD40	MD37	MD4	MD34	MD0	ADS#	NA#	CACHE	HA26	HA29	HA18	HA15	HA11	HA6	BE7#	BE2#	HD62	HD58	HD54	HD49	HD45	HD41	HD38	HD33	HD32
AE	MD39	MD38	MD5	MD35	MD2	EADS#	D/C#	BOFF#	AHOLD	HA24	HA31	HA19	HA16	HA12	HA5	HA10	BE3#	HD63	HD59	HD55	HD50	HD46	HD42	HD39	HD36	HD34
AF	MD7	MD6	MD36	MD3	HLOCK#	W/R#	HITM#	SMIACT#	KEN#	HA23	HA21	HA22	HA20	HA13	HA4	HA9	BE4#	BE0#	HD60	HD56	HD51	HD47	HD43	HD40	HD37	HD35

Figure 3. VT82C597 Pin List (Numerical Order)

Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Names	Pin #		Pin Name
A01	IO	MD58	D02	IO	MD54	H25	O	GNT3#	P02	O	MA10	W05	IO	MPD1	AD02	IO	MD40
A02	IO	MD27	D03	IO	MD23	H26	IO	AD14	P03	O	MA11	W22	IO	HD14	AD03	IO	MD37
A03	IO	MD28	D04	IO	MD55	J01	O	CAS7# / DQM7#	P04	O	MA04	W23	IO	HD13	AD04	IO	MD04
A04	IO	MD61	D05	IO	MD30	J02	O	SWEA# / MWEA#	P05	P	**MVREF**	W24	IO	HD12	AD05	IO	MD34
A05	IO	MD63	D06	IO	GD08	J03	O	SWEB# / MWEB#	P11	P	**GND**	W25	IO	HD11	AD06	IO	MD00
A06	IO	GD01	D07	IO	GD03	J04	IO	MPD3	P12	P	**GND**	W26	IO	HD10	AD07	IO	ADS#
A07	IO	GD07	D08	P	**GND**	J05	P	**MVCC**	P13	P	**GND**	Y01	IO	MD46	AD08	O	NA#
A08	IO	GBE0#	D09	IO	GD10	J09	P	**GND**	P14	P	**GND**	Y02	IO	MD15	AD09	I	CACHE#
A09	IO	GD11	D10	IO	GD14	J14	P	**GND**	P15	P	**GND**	Y03	IO	MD47	AD10	IO	HA26
A10	IO	GBE1#	D11	IO	GBE2#	J18	P	**GND**	P16	P	**GND**	Y04	IO	MPD4	AD11	IO	HA29
A11	IO	GTRDY#	D12	IO	GD21	J22	P	**PVCC**	P17	P	**GND**	Y05	P	**GND**	AD12	IO	HA18
A12	IO	GD17	D13	IO	GD23	J23	IO	AD08	P18	P	**GND**	Y22	IO	HD19	AD13	IO	HA15
A13	IO	GD20	D14	IO	GDS1#	J24	IO	AD15	P22	P	**GND**	Y23	IO	HD18	AD14	IO	HA11
A14	IO	GD25	D15	IO	GD27	J25	IO	CBE1#	P23	IO	TA8	Y24	IO	HD17	AD15	IO	HA06
A15	IO	GD28	D16	I	SBA6	J26	IO	DEVSEL#	P24	O	TWE#	Y25	IO	HD16	AD16	IO	BE7#
A16	IO	GD31	D17	I	SBA2	K01	O	CAS1# / DQM1#	P25	IO	TA6	Y26	IO	HD15	AD17	IO	BE2#
A17	I	SBA5	D18	I	SBA0	K02	O	CAS5# / DQM5#	P26	IO	TA7	AA01	IO	MD13	AD18	IO	HD62
A18	I	SBA1	D19	I	PCLK	K03	O	CAS3# / DQM3#	R01	O	MA05	AA02	IO	MD45	AD19	IO	HD58
A19	O	ST0	D20	IO	PAR	K04	IO	MPD2	R02	O	MA06	AA03	IO	MD14	AD20	IO	HD54
A20	I	GREQ#	D21	O	ST2	K05	P	**AGND**	R03	O	MA07	AA04	IO	MPD0	AD21	IO	HD49
A21	IO	GPAR	D22	IO	AD00	K10	P	**GND**	R04	O	MAB0	AA05	P	**GND**	AD22	IO	HD45
A22	IO	STOP#	D23	IO	AD01	K14	P	**GND**	R05	P	**MVCC**	AA22	P	**GND**	AD23	IO	HD41
A23	IO	AD17	D24	IO	AD27	K17	P	**GND**	R11	P	**GND**	AA23	IO	HD23	AD24	IO	HD38
A24	IO	AD21	D25	IO	AD26	K22	P	**PVCC**	R12	P	**GND**	AA24	IO	HD22	AD25	IO	HD33
A25	IO	AD22	D26	IO	AD28	K23	IO	CBE0#	R13	P	**GND**	AA25	IO	HD21	AD26	IO	HD32
A26	IO	AD23	E01	IO	MD52	K24	IO	AD09	R14	P	**GND**	AA26	IO	HD20	AE01	IO	MD39
B01	IO	MD57	E02	IO	MD21	K25	IO	TRDY#	R15	P	**GND**	AB01	IO	MD43	AE02	IO	MD38
B02	IO	MD26	E03	IO	MD53	K26	IO	IRDY#	R16	P	**GND**	AB02	IO	MD12	AE03	IO	MD05
B03	IO	MD59	E04	O	DS3#	L01	O	RAS3# / CS3#	R22	P	**GND**	AB03	IO	MD44	AE04	IO	MD35
B04	IO	MD29	E05	P	**CVCC**	L02	O	RAS1# / CS1#	R23	O	BWE#	AB04	IO	MD11	AE05	IO	MD02
B05	IO	MD31	E06	P	**GND**	L03	O	RAS0# / CS0#	R24	O	CCS1#	AB05	P	**CVCC**	AE06	O	EADS#
B06	IO	GD00	E07	P	**GND**	L04	IO	MPD6	R25	O	COE1#	AB06	P	**MVCC**	AE07	IO	D/C#
B07	IO	GD04	E08	I	GCLK	L05	P	**GND**	R26	IO	TA9	AB07	P	**MVCC**	AE08	O	BOFF#
B08	IO	GDS0#	E09	P	**GVCC**	L11	P	**GND**	T01	O	MAB1	AB08	P	**5VREF**	AE09	O	AHOLD
B09	IO	GD12	E10	P	**GVCC**	L12	P	**GND**	T02	O	MA02	AB09	P	**HVCC**	AE10	IO	HA24
B10	IO	GD15	E11	P	**GVCC**	L13	P	**GND**	T03	O	MA03	AB10	P	**HVCC**	AE11	IO	HA31
B11	IO	GDSEL#	E12	IO	GD16	L14	P	**GND**	T04	O	CAS2# / DQM2#	AB11	IO	HA25	AE12	IO	HA19
B12	IO	GFRM#	E13	P	**GVREF**	L15	P	**GND**	T05	P	**MVCC**	AB12	IO	HA30	AE13	IO	HA16
B13	IO	GD19	E14	P	**GND**	L16	P	**GND**	T11	P	**GND**	AB13	P	**GND**	AE14	IO	HA12
B14	IO	GBE3#	E15	P	**GND**	L22	P	**PVCC**	T12	P	**GND**	AB14	P	**GND**	AE15	IO	HA05
B15	IO	GD26	E16	P	**GND**	L23	IO	AD10	T13	P	**GND**	AB15	IO	HA08	AE16	IO	HA10
B16	IO	GD29	E17	P	**GVCC**	L24	IO	AD12	T14	P	**GND**	AB16	IO	BE5#	AE17	IO	BE3#
B17	I	SBA4	E18	P	**GVCC**	L25	IO	FRAME#	T15	P	**GND**	AB17	P	**HVCC**	AE18	IO	HD63
B18	I	SBA3	E19	P	**GVCC**	L26	O	PGNT#	T16	P	**GND**	AB18	P	**HVCC**	AE19	IO	HD59
B19	I	GPIPE#	E20	-	Reserved	M01	O	MAA1	T22	IO	HD01	AB19	P	**HVCC**	AE20	IO	HD55
B20	O	ST1	E21	P	**5VREF**	M02	O	RAS5# / CS5#	T23	IO	HD00	AB20	IO	HD52	AE21	IO	HD50
B21	O	GGNT#	E22	P	**GND**	M03	O	RAS4# / CS4#	T24	O	CADV#	AB21	P	**CVCC**	AE22	IO	HD46
B22	IO	LOCK#	E23	IO	AD02	M04	O	RAS2# / CS2#	T25	O	CADS#	AB22	P	**GND**	AE23	IO	HD42
B23	IO	AD16	E24	IO	AD29	M05	P	**GND**	T26	O	GWE#	AB23	IO	HD27	AE24	IO	HD39
B24	IO	AD19	E25	IO	AD30	M11	P	**GND**	U01	O	SRASC#	AB24	IO	HD26	AE25	IO	HD36
B25	IO	AD20	E26	IO	AD31	M12	P	**GND**	U02	O	SRASB#	AB25	IO	HD25	AE26	IO	HD34
B26	IO	CBE3#	F01	IO	MD19	M13	P	**GND**	U03	O	SRASA#	AB26	IO	HD24	AF01	IO	MD07
C01	IO	MD24	F02	IO	MD51	M14	P	**GND**	U04	O	DS0#	AC01	IO	MD41	AF02	IO	MD06
C02	IO	MD56	F03	IO	MD20	M15	P	**GND**	U05	P	**MVCC**	AC02	IO	MD10	AF03	IO	MD36
C03	IO	MD25	F04	O	DS1#	M16	P	**GND**	U10	P	**GND**	AC03	IO	MD42	AF04	IO	MD03
C04	IO	MD60	F05	P	**AVCC**	M22	IO	AD11	U13	P	**GND**	AC04	IO	MD9	AF05	I	HLOCK#
C05	IO	MD62	F22	P	**CVCC**	M23	IO	AD13	U17	P	**GND**	AC05	IO	MD33	AF06	IO	W/R#
C06	IO	GD05	F23	IO	AD03	M24	I	PREQ#	U22	P	**HVCC**	AC06	IO	MD32	AF07	I	HITM#
C07	IO	GD02	F24	I	REQ0#	M25	I	RESET#	U23	IO	HD05	AC07	IO	MD01	AF08	I	SMIACT#
C08	IO	GD06	F25	O	GNT0#	M26	IO	TA2	U24	IO	HD04	AC08	IO	BRDY#	AF09	O	KEN#
C09	IO	GD09	F26	I	REQ1#	N01	O	MA12	U25	IO	HD03	AC09	IO	M/IO#	AF10	IO	HA23
C10	IO	GD13	G01	IO	MD49	N02	O	MA13	U26	IO	HD02	AC10	IO	HA27	AF11	IO	HA21
C11	IO	GSTOP#	G02	IO	MD18	N03	O	MAA0	V01	O	CAS0# / DQM0#	AC11	IO	HA28	AF12	IO	HA22
C12	IO	GIRDY#	G03	IO	MD50	N04	O	MA08	V02	O	CAS4# / DQM4#	AC12	IO	HA17	AF13	IO	HA20
C13	IO	GD18	G04	IO	MD17	N05	I	HCLK	V03	O	CAS6# / DQM6#	AC13	IO	HA14	AF14	IO	HA13
C14	IO	GD22	G05	P	**MVCC**	N09	P	**GND**	V04	O	DS2#	AC14	IO	HA03	AF15	IO	HA04
C15	IO	GD24	G22	IO	AD05	N10	P	**GND**	V05	P	**MVCC**	AC15	IO	HA07	AF16	IO	HA09
C16	IO	GD30	G23	IO	AD04	N11	P	**GND**	V09	P	**GND**	AC16	IO	BE6#	AF17	IO	BE4#
C17	I	SBA7	G24	O	GNT1#	N12	P	**GND**	V13	P	**GND**	AC17	IO	BE1#	AF18	IO	BE0#
C18	I	SBS#	G25	I	REQ2#	N13	P	**GND**	V18	P	**GND**	AC18	IO	HD61	AF19	IO	HD60
C19	I	GRBF#	G26	O	GNT2#	N14	P	**GND**	V22	P	**HVCC**	AC19	IO	HD57	AF20	IO	HD56
C20	IO	GSERR#	H01	O	SWEC# / MWEC#	N15	P	**GND**	V23	IO	HD09	AC20	IO	HD53	AF21	IO	HD51
C21	-	Reserved	H02	IO	MD16	N16	P	**GND**	V24	IO	HD08	AC21	IO	HD48	AF22	IO	HD47
C22	IO	SERR#	H03	IO	MD48	N22	IO	TA5	V25	IO	HD07	AC22	IO	HD44	AF23	IO	HD43
C23	IO	CBE2#	H04	IO	MPD7	N23	IO	TA4	V26	IO	HD06	AC23	IO	HD31	AF24	IO	HD40
C24	IO	AD18	H05	P	**MVCC**	N24	IO	TA3	W01	O	SCASC#	AC24	IO	HD30	AF25	IO	HD37
C25	IO	AD24	H22	IO	AD06	N25	IO	TA0	W02	O	SCASB#	AC25	IO	HD29	AF26	IO	HD35
C26	IO	AD25	H23	IO	AD07	N26	IO	TA1	W03	O	SCASA#	AC26	IO	HD28			
D01	IO	MD22	H24	I	REQ3#	P01	O	MA09	W04	IO	MPD5	AD01	IO	MD8			

Figure 4. VT82C597 Pin List (Alphabetical Order)

Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Names	Pin #		Pin Name
AB08	P	**5VREF**	L25	IO	FRAME#	P13	P	**GND**	AE11	IO	HA31	T02	O	MA02	A05	IO	MD63
E21	P	**5VREF**	A08	IO	GBE0#	P14	P	**GND**	N05	I	HCLK	T03	O	MA03	AA04	IO	MPD0
D22	IO	AD00	A10	IO	GBE1#	P15	P	**GND**	T23	IO	HD00	P04	O	MA04	W05	IO	MPD1
D23	IO	AD01	D11	IO	GBE2#	P16	P	**GND**	T22	IO	HD01	R01	O	MA05	K04	IO	MPD2
E23	IO	AD02	B14	IO	GBE3#	P17	P	**GND**	U26	IO	HD02	R02	O	MA06	J04	IO	MPD3
F23	IO	AD03	E08	I	GCLK	P18	P	**GND**	U25	IO	HD03	R03	O	MA07	Y04	IO	MPD4
G23	IO	AD04	B06	IO	GD00	P22	P	**GND**	U24	IO	HD04	N04	O	MA08	W04	IO	MPD5
G22	IO	AD05	A06	IO	GD01	R11	P	**GND**	U23	IO	HD05	P01	O	MA09	L04	IO	MPD6
H22	IO	AD06	C07	IO	GD02	R12	P	**GND**	V26	IO	HD06	P02	O	MA10	H04	IO	MPD7
H23	IO	AD07	D07	IO	GD03	R13	P	**GND**	V25	IO	HD07	P03	O	MA11	G05	P	**MVCC**
J23	IO	AD08	B07	IO	GD04	R14	P	**GND**	V24	IO	HD08	N01	O	MA12	H05	P	**MVCC**
K24	IO	AD09	C06	IO	GD05	R15	P	**GND**	V23	IO	HD09	N02	O	MA13	J05	P	**MVCC**
L23	IO	AD10	C08	IO	GD06	R16	P	**GND**	W26	IO	HD10	N03	O	MAA0	R05	P	**MVCC**
M22	IO	AD11	A07	IO	GD07	R22	P	**GND**	W25	IO	HD11	M01	O	MAA1	T05	P	**MVCC**
L24	IO	AD12	D06	IO	GD08	T11	P	**GND**	W24	IO	HD12	R04	O	MAB0	U05	P	**MVCC**
M23	IO	AD13	C09	IO	GD09	T12	P	**GND**	W23	IO	HD13	T01	O	MAB1	V05	P	**MVCC**
H26	IO	AD14	D09	IO	GD10	T13	P	**GND**	W22	IO	HD14	AD06	IO	MD00	AB06	P	**MVCC**
J24	IO	AD15	A09	IO	GD11	T14	P	**GND**	Y26	IO	HD15	AC07	IO	MD01	AB07	P	**MVCC**
B23	IO	AD16	B09	IO	GD12	T15	P	**GND**	Y25	IO	HD16	AE05	IO	MD02	P05	P	**MVREF**
A23	IO	AD17	C10	IO	GD13	T16	P	**GND**	Y24	IO	HD17	AF04	IO	MD03	AD08	O	NA#
C24	IO	AD18	D10	IO	GD14	U10	P	**GND**	Y23	IO	HD18	AD04	IO	MD04	D20	IO	PAR
B24	IO	AD19	B10	IO	GD15	U13	P	**GND**	Y22	IO	HD19	AE03	IO	MD05	D19	I	PCLK
B25	IO	AD20	E12	IO	GD16	U17	P	**GND**	AA26	IO	HD20	AF02	IO	MD06	L26	O	PGNT#
A24	IO	AD21	A12	IO	GD17	V09	P	**GND**	AA25	IO	HD21	AF01	IO	MD07	M24	I	PREQ#
A25	IO	AD22	C13	IO	GD18	V13	P	**GND**	AA24	IO	HD22	AD01	IO	MD08	J22	P	**PVCC**
A26	IO	AD23	B13	IO	GD19	V18	P	**GND**	AA23	IO	HD23	AC04	IO	MD09	K22	P	**PVCC**
C25	IO	AD24	A13	IO	GD20	Y05	P	**GND**	AB26	IO	HD24	AC02	IO	MD10	L22	P	**PVCC**
C26	IO	AD25	D12	IO	GD21	AA05	P	**GND**	AB25	IO	HD25	AB04	IO	MD11	L03	O	RAS0# / CS0#
D25	IO	AD26	C14	IO	GD22	AA22	P	**GND**	AB24	IO	HD26	AB02	IO	MD12	L02	O	RAS1# / CS1#
D24	IO	AD27	D13	IO	GD23	AB13	P	**GND**	AB23	IO	HD27	AA01	IO	MD13	M04	O	RAS2# / CS2#
D26	IO	AD28	C15	IO	GD24	AB14	P	**GND**	AC26	IO	HD28	AA03	IO	MD14	L01	O	RAS3# / CS3#
E24	IO	AD29	A14	IO	GD25	AB22	P	**GND**	AC25	IO	HD29	Y02	IO	MD15	M03	O	RAS4# / CS4#
E25	IO	AD30	B15	IO	GD26	F25	O	GNT0#	AC24	IO	HD30	H02	IO	MD16	M02	O	RAS5# / CS5#
E26	IO	AD31	D15	IO	GD27	G24	O	GNT1#	AC23	IO	HD31	G04	IO	MD17	F24	I	REQ0#
AD07	IO	ADS#	A15	IO	GD28	G26	O	GNT2#	AD26	IO	HD32	G02	IO	MD18	F26	I	REQ1#
B08	IO	GDS0#	B16	IO	GD29	H25	O	GNT3#	AD25	IO	HD33	F01	IO	MD19	G25	I	REQ2#
D14	IO	GDS1#	C16	IO	GD30	A21	IO	GPAR	AE26	IO	HD34	F03	IO	MD20	H24	I	REQ3#
K05	P	**AGND**	A16	IO	GD31	B19	I	GPIPE#	AF26	IO	HD35	E02	IO	MD21	C21	-	Reserved
AE09	O	AHOLD	B11	IO	GDSEL#	C19	I	GRBF#	AE25	IO	HD36	D01	IO	MD22	E20	-	Reserved
F05	P	**AVCC**	B12	IO	GFRM#	A20	I	GREQ#	AF25	IO	HD37	D03	IO	MD23	M25	I	RESET#
AF18	IO	BE0#	B21	O	GGNT#	C20	IO	GSERR#	AD24	IO	HD38	C01	IO	MD24	D18	I	SBA0
AC17	IO	BE1#	C12	IO	GIRDY#	C11	IO	GSTOP#	AE24	IO	HD39	C03	IO	MD25	A18	I	SBA1
AD17	IO	BE2#	D08	P	**GND**	A11	IO	GTRDY#	AF24	IO	HD40	B02	IO	MD26	D17	I	SBA2
AE17	IO	BE3#	E06	P	**GND**	E09	P	**GVCC**	AD23	IO	HD41	A02	IO	MD27	B18	I	SBA3
AF17	IO	BE4#	E07	P	**GND**	E10	P	**GVCC**	AE23	IO	HD42	A03	IO	MD28	B17	I	SBA4
AB16	IO	BE5#	E14	P	**GND**	E11	P	**GVCC**	AF23	IO	HD43	B04	IO	MD29	A17	I	SBA5
AC16	IO	BE6#	E15	P	**GND**	E17	P	**GVCC**	AC22	IO	HD44	D05	IO	MD30	D16	I	SBA6
AD16	IO	BE7#	E16	P	**GND**	E18	P	**GVCC**	AD22	IO	HD45	B05	IO	MD31	C17	I	SBA7
AE08	O	BOFF#	E22	P	**GND**	E19	P	**GVCC**	AE22	IO	HD46	AC06	IO	MD32	C18	I	SBS#
AC08	IO	BRDY#	J09	P	**GND**	E13	P	**GVREF**	AF22	IO	HD47	AC05	IO	MD33	W03	O	SCASA#
R23	O	BWE#	J14	P	**GND**	T26	O	GWE#	AC21	IO	HD48	AD05	IO	MD34	W02	O	SCASB#
AD09	I	CACHE#	J18	P	**GND**	AC14	IO	HA03	AD21	IO	HD49	AE04	IO	MD35	W01	O	SCASC#
T25	O	CADS#	K10	P	**GND**	AF15	IO	HA04	AE21	IO	HD50	AF03	IO	MD36	C22	IO	SERR#
T24	O	CADV#	K14	P	**GND**	AE15	IO	HA05	AF21	IO	HD51	AD03	IO	MD37	AF08	I	SMIACT#
V01	O	CAS0# / DQM0#	K17	P	**GND**	AD15	IO	HA06	AB20	IO	HD52	AE02	IO	MD38	U03	O	SRASA#
K01	O	CAS1# / DQM1#	L05	P	**GND**	AC15	IO	HA07	AC20	IO	HD53	AE01	IO	MD39	U02	O	SRASB#
T04	O	CAS2# / DQM2#	L11	P	**GND**	AB15	IO	HA08	AD20	IO	HD54	AD02	IO	MD40	U01	O	SRASC#
K03	O	CAS3# / DQM3#	L12	P	**GND**	AF16	IO	HA09	AE20	IO	HD55	AC01	IO	MD41	A19	O	ST0
V02	O	CAS4# / DQM4#	L13	P	**GND**	AE16	IO	HA10	AF20	IO	HD56	AC03	IO	MD42	B20	O	ST1
K02	O	CAS5# / DQM5#	L14	P	**GND**	AD14	IO	HA11	AC19	IO	HD57	AB01	IO	MD43	D21	O	ST2
V03	O	CAS6# / DQM6#	L15	P	**GND**	AE14	IO	HA12	AD19	IO	HD58	AB03	IO	MD44	A22	IO	STOP#
J01	O	CAS7# / DQM7#	L16	P	**GND**	AF14	IO	HA13	AE19	IO	HD59	AA02	IO	MD45	J02	O	SWEA# / MWEA#
K23	IO	CBE0#	M05	P	**GND**	AC13	IO	HA14	AF19	IO	HD60	Y01	IO	MD46	J03	O	SWEB# / MWEB#
J25	IO	CBE1#	M11	P	**GND**	AD13	IO	HA15	AC18	IO	HD61	Y03	IO	MD47	H01	O	SWEC# / MWEC#
C23	IO	CBE2#	M12	P	**GND**	AE13	IO	HA16	AD18	IO	HD62	H03	IO	MD48	N25	IO	TA0
B26	IO	CBE3#	M13	P	**GND**	AC12	IO	HA17	AE18	IO	HD63	G01	IO	MD49	N26	IO	TA1
R24	O	CCS1#	M14	P	**GND**	AD12	IO	HA18	AF07	I	HITM#	G03	IO	MD50	M26	IO	TA2
R25	O	COE1#	M15	P	**GND**	AE12	IO	HA19	AF05	I	HLOCK#	F02	IO	MD51	N24	IO	TA3
E05	P	**CVCC**	M16	P	**GND**	AF13	IO	HA20	AB09	P	**HVCC**	E01	IO	MD52	N23	IO	TA4
F22	P	**CVCC**	N09	P	**GND**	AF11	IO	HA21	AB10	P	**HVCC**	E03	IO	MD53	N22	IO	TA5
AB05	P	**CVCC**	N10	P	**GND**	AF12	IO	HA22	AB17	P	**HVCC**	D02	IO	MD54	P25	IO	TA6
AB21	P	**CVCC**	N11	P	**GND**	AF10	IO	HA23	AB18	P	**HVCC**	D04	IO	MD55	P26	IO	TA7
AE07	IO	D/C#	N12	P	**GND**	AE10	IO	HA24	AB19	P	**HVCC**	C02	IO	MD56	P23	IO	TA8
J26	IO	DEVSEL#	N13	P	**GND**	AB11	IO	HA25	U22	P	**HVCC**	B01	IO	MD57	R26	IO	TA9
U04	O	DS0#	N14	P	**GND**	AD10	IO	HA26	V22	P	**HVCC**	A01	IO	MD58	K25	IO	TRDY#
F04	O	DS1#	N15	P	**GND**	AC10	IO	HA27	K26	IO	IRDY#	B03	IO	MD59	P24	O	TWE#
V04	O	DS2#	N16	P	**GND**	AC11	IO	HA28	AF09	O	KEN#	C04	IO	MD60	AF06	IO	W/R#
E04	O	DS3#	P11	P	**GND**	AD11	IO	HA29	B22	IO	LOCK#	A04	IO	MD61			
AE06	O	EADS#	P12	P	**GND**	AB12	IO	HA30	AC09	IO	M/IO#	C05	IO	MD62			

PINOUTS

Figure 5. VT82C597AT Ball Diagram (Top View)

Key	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	SBA5	SBA3	GPIPE#	GREQ#	GSERR#	SBA0	MD0	MD33	MD35	MD37	MD39	MD41	MD12	MD46	MPD4	SCASC#	CAS0#	SRASC#	MAB1	MA5	MA9	MA13	RAS4#	RAS1#	CAS2#	CAS3#
B	SBA6	SBS#	GRBF#	ST1	GGNT#	GPAR	MD32	MD2	MD4	MD6	MD8	MD10	MD44	MD15	MPD1	SCASB#	CAS4#	SRASB#	MA2	MA6	MA10	MAA0	RAS3#	RAS0#	CAS6#	CAS7#
C	GD31	SBA7	SBA1	ST0	SBA2	-res-	MD1	MD34	MD36	MD38	MD40	MD42	MD13	MD47	MPD5	SCASA#	CAS5#	SRASA#	MA3	MA7	MA11	MAA1	RAS2#	SWEC#	SWEB#	SWEA#
D	GD28	GD30	GD29	GCLK	SBA4	-res-	MD3	**GND**	MD5	MD7	MD9	MD11	MD45	MPD0	DS0#	DS2#	CAS1#	MAB0	MA4	MA8	MA12	RAS5#	MPD7	MPD3	MPD6	MPD2
E	GD24	GD26	GDS1#	GD27	**CVCC**	**GND**	**GND**	ST2	**MVCC**	**MVCC**	**MVCC**	MD43	MD14	**GND**	**GND**	**GND**	**MVCC**	**MVCC**	**MVCC**	**MVREF**	**5VREF**	**GND**	MD49	MD17	MD48	MD16
F	GBE3#	GD25	GD21	GD23	**GVREF**	**F6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**F21**	**CVCC**	MD51	MD19	MD50	MD18
G	GD20	GD22	GBE2#	GD17	**GVCC**	**G**			**Total = 472 Pins**				**Data**			**Control**			**Address**	**Control**	**G**	DS1#	MD53	MD21	MD52	MD20
H	GD16	GD18	GD19	GDSEL#	**GVCC**	**H**	**AGP**		**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**		**Data**	**H**	DS3#	MD55	MD23	MD54	MD22
J	GTRDY#	GIRDY#	GFRM#	GBE1#	**GVCC**	**J**	**Pins**	**J**	**GND**					**GND**				**GND**	**J**	**Mem**	**J**	**MVCC**	MD57	MD25	MD56	MD24
K	GD13	GD15	GSTOP#	GD14	**AVCC**	**K**		**K**		**GND**	**11**	**12**	**13**	**GND**	**15**	**16**	**GND**		**K**	**Pins**	**K**	**MVCC**	MD59	MD27	MD58	MD26
L	GD9	GD12	GD11	GD10	**GND**	**L**		**L**		**L**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**			**L**		**L**	**MVCC**	MD61	MD29	MD60	MD28
M	GD6	GD8	GBE0#	GDS0#	**GND**	**M**		**M**		**M**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**			**M**		**M**	TA2	MD63	MD31	MD62	MD30
N	GD2	GD4	GD7	GD5	**AGND**	**N**		**N**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**			**N**		**N**	TA5	TA4	TA3	TA0	TA1
P	GD3	GD1	GD0	GNT3#	HCLK	**P**		**P**		**P**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**P**	**Cache**	**P**	**GND**	TA8	TWE#	TA6	TA7
R	GNT1#	REQ2#	GNT2#	REQ3#	**PVCC**	**R**		**R**		**R**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**			**R**		**R**	**GND**	BWE#	CCS1#	COE1#	TA9
T	LOCK#	REQ0#	GNT0#	REQ1#	**PVCC**	**T**		**T**		**T**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**			**T**		**T**	HD1	HD0	CADV#	CADS#	GWE#
U	AD28	AD29	AD30	AD31	**PVCC**	**U**		**U**		**GND**			**GND**				**GND**		**U**		**U**	**HVCC**	HD5	HD4	HD3	HD2
V	AD24	AD25	AD26	AD27	**PVCC**	**V**	**PCI**	**V**	**GND**				**GND**					**GND**	**V**		**V**	**HVCC**	HD9	HD8	HD7	HD6
W	AD21	AD22	AD23	CBE3#	PCLK	**W**	**Pins**		**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**		**Data**	**W**	HD14	HD13	HD12	HD11	HD10
Y	AD17	AD18	AD19	AD20	**GND**	**Y**			**Control**			**Address**		**CPU Pins**		**Byte Enables**					**Y**	HD19	HD18	HD17	HD16	HD15
AA	IRDY#	FRM#	CBE2#	AD16	**GND**	**AA6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**AA21**	**GND**	HD23	HD22	HD21	HD20
AB	STOP#	DSEL#	TRDY#	SERR#	**CVCC**	**PVCC**	**PVCC**	**5VREF**	**HVCC**	**HVCC**	HA25	HA30	**GND**	**GND**	HA8	BE5#	**HVCC**	**HVCC**	**HVCC**	HD52	**CVCC**	**GND**	HD27	HD26	HD25	HD24
AC	CBE1#	PAR	AD15	AD14	AD2	PREQ#	RESET#	BRDY#	M/IO#	HA27	HA28	HA17	HA14	HA3	HA7	BE6#	BE1#	HD61	HD57	HD53	HD48	HD44	HD31	HD30	HD29	HD28
AD	AD13	AD12	AD11	AD5	AD1	PGNT#	ADS#	NA#	CACHE#	HA26	HA29	HA18	HA15	HA11	HA6	BE7#	BE2#	HD62	HD58	HD54	HD49	HD45	HD41	HD38	HD33	HD32
AE	AD10	AD9	AD7	AD4	AD0	EADS#	D/C#	BOFF#	AHOLD	HA24	HA31	HA19	HA16	HA12	HA5	HA10	BE3#	HD63	HD59	HD55	HD50	HD46	HD42	HD39	HD36	HD34
AF	AD8	CBE0#	AD6	AD3	HLOCK#	W/R#	HITM#	SMIACT#	KEN#	HA23	HA21	HA22	HA20	HA13	HA4	HA9	BE4#	BE0#	HD60	HD56	HD51	HD47	HD43	HD40	HD37	HD35

Figure 6. VT82C597AT Pin List (Numerical Order)

Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Names	Pin #		Pin Name
A01	I	SBA5	D02	IO	GD30	H25	IO	MD54	P02	IO	GD01	W05	I	PCLK	AD02	IO	AD12
A02	I	SBA3	D03	IO	GD29	H26	IO	MD22	P03	IO	GD00	W22	IO	HD14	AD03	IO	AD11
A03	I	GPIPE#	D04	I	GCLK	J01	IO	GTRDY#	P04	O	GNT3#	W23	IO	HD13	AD04	IO	AD05
A04	I	GREQ#	D05	I	SBA4	J02	IO	GIRDY#	P05	I	HCLK	W24	IO	HD12	AD05	IO	AD01
A05	IO	GSERR#	D06	-	Reserved	J03	IO	GFRM#	P11	P	**GND**	W25	IO	HD11	AD06	O	PGNT#
A06	I	SBA0	D07	IO	MD03	J04	IO	GBE1#	P12	P	**GND**	W26	IO	HD10	AD07	IO	ADS#
A07	IO	MD00	D08	P	**GND**	J05	P	**GVCC**	P13	P	**GND**	Y01	IO	AD17	AD08	O	NA#
A08	IO	MD33	D09	IO	MD05	J09	P	**GND**	P14	P	**GND**	Y02	IO	AD18	AD09	I	CACHE#
A09	IO	MD35	D10	IO	MD07	J14	P	**GND**	P15	P	**GND**	Y03	IO	AD19	AD10	IO	HA26
A10	IO	MD37	D11	IO	MD09	J18	P	**GND**	P16	P	**GND**	Y04	IO	AD20	AD11	IO	HA29
A11	IO	MD39	D12	IO	MD11	J22	P	**MVCC**	P17	P	**GND**	Y05	P	**GND**	AD12	IO	HA18
A12	IO	MD41	D13	IO	MD45	J23	IO	MD57	P18	P	**GND**	Y22	IO	HD19	AD13	IO	HA15
A13	IO	MD12	D14	IO	MPD0	J24	IO	MD25	P22	P	**GND**	Y23	IO	HD18	AD14	IO	HA11
A14	IO	MD46	D15	O	DS0#	J25	IO	MD56	P23	IO	TA8	Y24	IO	HD17	AD15	IO	HA06
A15	IO	MPD4	D16	O	DS2#	J26	IO	MD24	P24	O	TWE#	Y25	IO	HD16	AD16	IO	BE7#
A16	O	SCASC#	D17	O	CAS1# / DQM1#	K01	IO	GD13	P25	IO	TA6	Y26	IO	HD15	AD17	IO	BE2#
A17	O	CAS0# / DQM0#	D18	O	MAB0	K02	IO	GD15	P26	IO	TA7	AA01	IO	IRDY#	AD18	IO	HD62
A18	O	SRASC#	D19	O	MA04	K03	IO	GSTOP#	R01	O	GNT1#	AA02	IO	FRAME#	AD19	IO	HD58
A19	O	MAB1	D20	O	MA08	K04	IO	GD14	R02	I	REQ2#	AA03	IO	CBE2#	AD20	IO	HD54
A20	O	MA05	D21	O	MA12	K05	P	**AVCC**	R03	O	GNT2#	AA04	IO	AD16	AD21	IO	HD49
A21	O	MA09	D22	O	RAS5# / CS5#	K10	P	**GND**	R04	I	REQ3#	AA05	P	**GND**	AD22	IO	HD45
A22	O	MA13	D23	IO	MPD7	K14	P	**GND**	R05	P	**PVCC**	AA22	P	**GND**	AD23	IO	HD41
A23	O	RAS4# / CS4#	D24	IO	MPD3	K17	P	**GND**	R11	P	**GND**	AA23	IO	HD23	AD24	IO	HD38
A24	O	RAS1# / CS1#	D25	IO	MPD6	K22	P	**MVCC**	R12	P	**GND**	AA24	IO	HD22	AD25	IO	HD33
A25	O	CAS2# / DQM2#	D26	IO	MPD2	K23	IO	MD59	R13	P	**GND**	AA25	IO	HD21	AD26	IO	HD32
A26	O	CAS3# / DQM3#	E01	IO	GD24	K24	IO	MD27	R14	P	**GND**	AA26	IO	HD20	AE01	IO	AD10
B01	I	SBA6	E02	IO	GD26	K25	IO	MD58	R15	P	**GND**	AB01	IO	STOP#	AE02	IO	AD09
B02	I	SBS#	E03	IO	GDS1#	K26	IO	MD26	R16	P	**GND**	AB02	IO	DEVSEL#	AE03	IO	AD07
B03	I	GRBF#	E04	IO	GD27	L01	IO	GD09	R22	P	**GND**	AB03	IO	TRDY#	AE04	IO	AD04
B04	O	ST1	E05	P	**CVCC**	L02	IO	GD12	R23	O	BWE#	AB04	IO	SERR#	AE05	IO	AD00
B05	O	GGNT#	E06	P	**GND**	L03	IO	GD11	R24	O	CCS1#	AB05	P	**CVCC**	AE06	O	EADS#
B06	IO	GPAR	E07	P	**GND**	L04	IO	GD10	R25	O	COE1#	AB06	P	**PVCC**	AE07	IO	D/C#
B07	IO	MD32	E08	O	ST2	L05	P	**GND**	R26	IO	TA9	AB07	P	**PVCC**	AE08	O	BOFF#
B08	IO	MD02	E09	P	**MVCC**	L11	P	**GND**	T01	IO	LOCK#	AB08	P	**5VREF**	AE09	O	AHOLD
B09	IO	MD04	E10	P	**MVCC**	L12	P	**GND**	T02	I	REQ0#	AB09	P	**HVCC**	AE10	IO	HA24
B10	IO	MD06	E11	P	**MVCC**	L13	P	**GND**	T03	O	GNT0#	AB10	P	**HVCC**	AE11	IO	HA31
B11	IO	MD08	E12	IO	MD43	L14	P	**GND**	T04	I	REQ1#	AB11	IO	HA25	AE12	IO	HA19
B12	IO	MD10	E13	IO	MD14	L15	P	**GND**	T05	P	**PVCC**	AB12	IO	HA30	AE13	IO	HA16
B13	IO	MD44	E14	P	**GND**	L16	P	**GND**	T11	P	**GND**	AB13	P	**GND**	AE14	IO	HA12
B14	IO	MD15	E15	P	**GND**	L22	P	**MVCC**	T12	P	**GND**	AB14	P	**GND**	AE15	IO	HA05
B15	IO	MPD1	E16	P	**GND**	L23	IO	MD61	T13	P	**GND**	AB15	IO	HA08	AE16	IO	HA10
B16	O	SCASB#	E17	P	**MVCC**	L24	IO	MD29	T14	P	**GND**	AB16	IO	BE5#	AE17	IO	BE3#
B17	O	CAS4# / DQM4#	E18	P	**MVCC**	L25	IO	MD60	T15	P	**GND**	AB17	P	**HVCC**	AE18	IO	HD63
B18	O	SRASB#	E19	P	**MVCC**	L26	IO	MD28	T16	P	**GND**	AB18	P	**HVCC**	AE19	IO	HD59
B19	O	MA02	E20	P	**MVREF**	M01	IO	GD06	T22	IO	HD01	AB19	P	**HVCC**	AE20	IO	HD55
B20	O	MA06	E21	P	**5VREF**	M02	IO	GD08	T23	IO	HD00	AB20	IO	HD52	AE21	IO	HD50
B21	O	MA10	E22	P	**GND**	M03	IO	GBE0#	T24	O	CADV#	AB21	P	**CVCC**	AE22	IO	HD46
B22	O	MAA0	E23	IO	MD49	M04	IO	GDS0#	T25	O	CADS#	AB22	P	**GND**	AE23	IO	HD42
B23	O	RAS3# / CS3#	E24	IO	MD17	M05	P	**GND**	T26	O	GWE#	AB23	IO	HD27	AE24	IO	HD39
B24	O	RAS0# / CS0#	E25	IO	MD48	M11	P	**GND**	U01	IO	AD28	AB24	IO	HD26	AE25	IO	HD36
B25	O	CAS6# / DQM6#	E26	IO	MD16	M12	P	**GND**	U02	IO	AD29	AB25	IO	HD25	AE26	IO	HD34
B26	O	CAS7# / DQM7#	F01	IO	GBE3#	M13	P	**GND**	U03	IO	AD30	AB26	IO	HD24	AF01	IO	AD08
C01	IO	GD31	F02	IO	GD25	M14	P	**GND**	U04	IO	AD31	AC01	IO	CBE1#	AF02	IO	CBE0#
C02	I	SBA7	F03	IO	GD21	M15	P	**GND**	U05	P	**PVCC**	AC02	IO	PAR	AF03	IO	AD06
C03	I	SBA1	F04	IO	GD23	M16	P	**GND**	U10	P	**GND**	AC03	IO	AD15	AF04	IO	AD03
C04	O	ST0	F05	P	**GVREF**	M22	IO	TA2	U13	P	**GND**	AC04	IO	AD14	AF05	I	HLOCK#
C05	I	SBA2	F22	P	**CVCC**	M23	IO	MD63	U17	P	**GND**	AC05	IO	AD02	AF06	IO	W/R#
C06	-	Reserved	F23	IO	MD51	M24	IO	MD31	U22	P	**HVCC**	AC06	I	PREQ#	AF07	I	HITM#
C07	IO	MD01	F24	IO	MD19	M25	IO	MD62	U23	IO	HD05	AC07	I	RESET#	AF08	I	SMIACT#
C08	IO	MD34	F25	IO	MD50	M26	IO	MD30	U24	IO	HD04	AC08	IO	BRDY#	AF09	O	KEN#
C09	IO	MD36	F26	IO	MD18	N01	IO	GD02	U25	IO	HD03	AC09	IO	M/IO#	AF10	IO	HA23
C10	IO	MD38	G01	IO	GD20	N02	IO	GD04	U26	IO	HD02	AC10	IO	HA27	AF11	IO	HA21
C11	IO	MD40	G02	IO	GD22	N03	IO	GD07	V01	IO	AD24	AC11	IO	HA28	AF12	IO	HA22
C12	IO	MD42	G03	IO	GBE2#	N04	IO	GD05	V02	IO	AD25	AC12	IO	HA17	AF13	IO	HA20
C13	IO	MD13	G04	IO	GD17	N05	P	**AGND**	V03	IO	AD26	AC13	IO	HA14	AF14	IO	HA13
C14	IO	MD47	G05	P	**GVCC**	N09	P	**GND**	V04	IO	AD27	AC14	IO	HA03	AF15	IO	HA04
C15	IO	MPD5	G22	O	DS1#	N10	P	**GND**	V05	P	**PVCC**	AC15	IO	HA07	AF16	IO	HA09
C16	O	SCASA#	G23	IO	MD53	N11	P	**GND**	V09	P	**GND**	AC16	IO	BE6#	AF17	IO	BE4#
C17	O	CAS5# / DQM5#	G24	IO	MD21	N12	P	**GND**	V13	P	**GND**	AC17	IO	BE1#	AF18	IO	BE0#
C18	O	SRASA#	G25	IO	MD52	N13	P	**GND**	V18	P	**GND**	AC18	IO	HD61	AF19	IO	HD60
C19	O	MA03	G26	IO	MD20	N14	P	**GND**	V22	P	**HVCC**	AC19	IO	HD57	AF20	IO	HD56
C20	O	MA07	H01	IO	GD16	N15	P	**GND**	V23	IO	HD09	AC20	IO	HD53	AF21	IO	HD51
C21	O	MA11	H02	IO	GD18	N16	P	**GND**	V24	IO	HD08	AC21	IO	HD48	AF22	IO	HD47
C22	O	MAA1	H03	IO	GD19	N22	IO	TA5	V25	IO	HD07	AC22	IO	HD44	AF23	IO	HD43
C23	O	RAS2# / CS2#	H04	IO	GDSEL#	N23	IO	TA4	V26	IO	HD06	AC23	IO	HD31	AF24	IO	HD40
C24	O	SWEC# / MWEC#	H05	P	**GVCC**	N24	IO	TA3	W01	IO	AD21	AC24	IO	HD30	AF25	IO	HD37
C25	O	SWEB# / MWEB#	H22	O	DS3#	N25	IO	TA0	W02	IO	AD22	AC25	IO	HD29	AF26	IO	HD35
C26	O	SWEA# / MWEA#	H23	IO	MD55	N26	IO	TA1	W03	IO	AD23	AC26	IO	HD28			
D01	IO	GD28	H24	IO	MD23	P01	IO	GD03	W04	IO	CBE3#	AD01	IO	AD13			

Figure 7. VT82C597AT Pin List (Alphabetical Order)

Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Names	Pin #		Pin Name
E21	P	**5VREF**	AA02	IO	FRAME#	P13	P	**GND**	T22	IO	HD01	A20	O	MA05	D26	IO	MPD2
AB08	P	**5VREF**	M03	IO	GBE0#	P14	P	**GND**	U26	IO	HD02	B20	O	MA06	D24	IO	MPD3
AE05	IO	AD00	J04	IO	GBE1#	P15	P	**GND**	U25	IO	HD03	C20	O	MA07	A15	IO	MPD4
AD05	IO	AD01	G03	IO	GBE2#	P16	P	**GND**	U24	IO	HD04	D20	O	MA08	C15	IO	MPD5
AC05	IO	AD02	F01	IO	GBE3#	P17	P	**GND**	U23	IO	HD05	A21	O	MA09	D25	IO	MPD6
AF04	IO	AD03	D04	I	GCLK	P18	P	**GND**	V26	IO	HD06	B21	O	MA10	D23	IO	MPD7
AE04	IO	AD04	P03	IO	GD00	P22	P	**GND**	V25	IO	HD07	C21	O	MA11	E09	P	**MVCC**
AD04	IO	AD05	P02	IO	GD01	R11	P	**GND**	V24	IO	HD08	D21	O	MA12	E10	P	**MVCC**
AF03	IO	AD06	N01	IO	GD02	R12	P	**GND**	V23	IO	HD09	A22	O	MA13	E11	P	**MVCC**
AE03	IO	AD07	P01	IO	GD03	R13	P	**GND**	W26	IO	HD10	B22	O	MAA0	E17	P	**MVCC**
AF01	IO	AD08	N02	IO	GD04	R14	P	**GND**	W25	IO	HD11	C22	O	MAA1	E18	P	**MVCC**
AE02	IO	AD09	N04	IO	GD05	R15	P	**GND**	W24	IO	HD12	D18	O	MAB0	E19	P	**MVCC**
AE01	IO	AD10	M01	IO	GD06	R16	P	**GND**	W23	IO	HD13	A19	O	MAB1	J22	P	**MVCC**
AD03	IO	AD11	N03	IO	GD07	R22	P	**GND**	W22	IO	HD14	A07	IO	MD00	K22	P	**MVCC**
AD02	IO	AD12	M02	IO	GD08	T11	P	**GND**	Y26	IO	HD15	C07	IO	MD01	L22	P	**MVCC**
AD01	IO	AD13	L01	IO	GD09	T12	P	**GND**	Y25	IO	HD16	B08	IO	MD02	E20	P	**MVREF**
AC04	IO	AD14	L04	IO	GD10	T13	P	**GND**	Y24	IO	HD17	D07	IO	MD03	AD08	O	NA#
AC03	IO	AD15	L03	IO	GD11	T14	P	**GND**	Y23	IO	HD18	B09	IO	MD04	AC02	IO	PAR
AA04	IO	AD16	L02	IO	GD12	T15	P	**GND**	Y22	IO	HD19	D09	IO	MD05	W05	I	PCLK
Y01	IO	AD17	K01	IO	GD13	T16	P	**GND**	AA26	IO	HD20	B10	IO	MD06	AD06	O	PGNT#
Y02	IO	AD18	K04	IO	GD14	U10	P	**GND**	AA25	IO	HD21	D10	IO	MD07	AC06	I	PREQ#
Y03	IO	AD19	K02	IO	GD15	U13	P	**GND**	AA24	IO	HD22	B11	IO	MD08	R05	P	**PVCC**
Y04	IO	AD20	H01	IO	GD16	U17	P	**GND**	AA23	IO	HD23	D11	IO	MD09	T05	P	**PVCC**
W01	IO	AD21	G04	IO	GD17	V09	P	**GND**	AB26	IO	HD24	B12	IO	MD10	U05	P	**PVCC**
W02	IO	AD22	H02	IO	GD18	V13	P	**GND**	AB21	IO	HD25	D12	IO	MD11	V05	P	**PVCC**
W03	IO	AD23	H03	IO	GD19	V18	P	**GND**	AB24	IO	HD26	A13	IO	MD12	AB06	P	**PVCC**
V01	IO	AD24	G01	IO	GD20	Y05	P	**GND**	AB23	IO	HD27	C13	IO	MD13	AB07	P	**PVCC**
V02	IO	AD25	F03	IO	GD21	AA05	P	**GND**	AC26	IO	HD28	E13	IO	MD14	B24	O	RAS0# / CS0#
V03	IO	AD26	G02	IO	GD22	AA22	P	**GND**	AC25	IO	HD29	B14	IO	MD15	A24	O	RAS1# / CS1#
V04	IO	AD27	F04	IO	GD23	AB13	P	**GND**	AC24	IO	HD30	E26	IO	MD16	C23	O	RAS2# / CS2#
U01	IO	AD28	E01	IO	GD24	AB14	P	**GND**	AC23	IO	HD31	E24	IO	MD17	B23	O	RAS3# / CS3#
U02	IO	AD29	F02	IO	GD25	AB22	P	**GND**	AD26	IO	HD32	F26	IO	MD18	A23	O	RAS4# / CS4#
U03	IO	AD30	E02	IO	GD26	T03	O	GNT0#	AD25	IO	HD33	F24	IO	MD19	D22	O	RAS5# / CS5#
U04	IO	AD31	E04	IO	GD27	R01	O	GNT1#	AE26	IO	HD34	G26	IO	MD20	T02	I	REQ0#
AD07	IO	ADS#	D01	IO	GD28	R03	O	GNT2#	AF26	IO	HD35	G24	IO	MD21	T04	I	REQ1#
M04	IO	GDS0#	D03	IO	GD29	P04	O	GNT3#	AE25	IO	HD36	H26	IO	MD22	R02	I	REQ2#
E03	IO	GDS1#	D02	IO	GD30	B06	IO	GPAR	AF25	IO	HD37	H24	IO	MD23	R04	I	REQ3#
N05	P	**AGND**	C01	IO	GD31	A03	I	GPIPE#	AD24	IO	HD38	J26	IO	MD24	C06	-	Reserved
AE09	O	AHOLD	H04	IO	GDSEL#	B03	I	GRBF#	AE24	IO	HD39	J24	IO	MD25	D06	-	Reserved
K05	P	**AVCC**	J03	IO	GFRM#	A04	I	GREQ#	AF24	IO	HD40	K26	IO	MD26	AC07	I	RESET#
AF18	IO	BE0#	B05	O	GGNT#	A05	IO	GSERR#	AD23	IO	HD41	K24	IO	MD27	A06	I	SBA0
AC17	IO	BE1#	J02	IO	GIRDY#	K03	IO	GSTOP#	AE23	IO	HD42	L26	IO	MD28	C03	I	SBA1
AD17	IO	BE2#	D08	P	**GND**	J01	IO	GTRDY#	AF23	IO	HD43	L24	IO	MD29	C05	I	SBA2
AE17	IO	BE3#	E06	P	**GND**	G05	P	**GVCC**	AC22	IO	HD44	M26	IO	MD30	A02	I	SBA3
AF17	IO	BE4#	E07	P	**GND**	H05	P	**GVCC**	AD22	IO	HD45	M24	IO	MD31	D05	I	SBA4
AB16	IO	BE5#	E14	P	**GND**	J05	P	**GVCC**	AE22	IO	HD46	B07	IO	MD32	A01	I	SBA5
AC16	IO	BE6#	E15	P	**GND**	F05	P	**GVREF**	AF22	IO	HD47	A08	IO	MD33	B01	I	SBA6
AD16	IO	BE7#	E16	P	**GND**	T26	O	GWE#	AC21	IO	HD48	C08	IO	MD34	C02	I	SBA7
AE08	O	BOFF#	E22	P	**GND**	AC14	IO	HA03	AD21	IO	HD49	A09	IO	MD35	B02	I	SBS#
AC08	IO	BRDY#	J09	P	**GND**	AF15	IO	HA04	AE21	IO	HD50	C09	IO	MD36	C16	O	SCASA#
R23	O	BWE#	J14	P	**GND**	AE15	IO	HA05	AF21	IO	HD51	A10	IO	MD37	B16	O	SCASB#
AD09	I	CACHE#	J18	P	**GND**	AD15	IO	HA06	AB20	IO	HD52	C10	IO	MD38	A16	O	SCASC#
T25	O	CADS#	K10	P	**GND**	AC15	IO	HA07	AC20	IO	HD53	A11	IO	MD39	AB04	IO	SERR#
T24	O	CADV#	K14	P	**GND**	AB15	IO	HA08	AD20	IO	HD54	C11	IO	MD40	AF08	I	SMIACT#
A17	O	CAS0# / DQM0#	K17	P	**GND**	AF16	IO	HA09	AE20	IO	HD55	A12	IO	MD41	C18	O	SRASA#
D17	O	CAS1# / DQM1#	L05	P	**GND**	AE16	IO	HA10	AF20	IO	HD56	C12	IO	MD42	B18	O	SRASB#
A25	O	CAS2# / DQM2#	L11	P	**GND**	AD14	IO	HA11	AC19	IO	HD57	E12	IO	MD43	A18	O	SRASC#
A26	O	CAS3# / DQM3#	L12	P	**GND**	AE14	IO	HA12	AD19	IO	HD58	B13	IO	MD44	C04	O	ST0
B17	O	CAS4# / DQM4#	L13	P	**GND**	AF14	IO	HA13	AE19	IO	HD59	D13	IO	MD45	B04	O	ST1
C17	O	CAS5# / DQM5#	L14	P	**GND**	AC13	IO	HA14	AF19	IO	HD60	A14	IO	MD46	E08	O	ST2
B25	O	CAS6# / DQM6#	L15	P	**GND**	AD13	IO	HA15	AC18	IO	HD61	C14	IO	MD47	AB01	IO	STOP#
B26	O	CAS7# / DQM7#	L16	P	**GND**	AE13	IO	HA16	AD18	IO	HD62	E25	IO	MD48	C26	O	SWEA# / MWEA#
AF02	IO	CBE0#	M05	P	**GND**	AC12	IO	HA17	AE18	IO	HD63	E23	IO	MD49	C25	O	SWEB# / MWEB#
AC01	IO	CBE1#	M11	P	**GND**	AD12	IO	HA18	AF07	I	HITM#	F25	IO	MD50	C24	O	SWEC# / MWEC#
AA03	IO	CBE2#	M12	P	**GND**	AE12	IO	HA19	AF05	I	HLOCK#	F23	IO	MD51	N25	IO	TA0
W04	IO	CBE3#	M13	P	**GND**	AF13	IO	HA20	U22	P	**HVCC**	G25	IO	MD52	N26	IO	TA1
R24	O	CCS1#	M14	P	**GND**	AF11	IO	HA21	V22	P	**HVCC**	G23	IO	MD53	M22	IO	TA2
R25	O	COE1#	M15	P	**GND**	AF12	IO	HA22	AB09	P	**HVCC**	H25	IO	MD54	N24	IO	TA3
E05	P	**CVCC**	M16	P	**GND**	AF10	IO	HA23	AB10	P	**HVCC**	H23	IO	MD55	N23	IO	TA4
F22	P	**CVCC**	N09	P	**GND**	AE10	IO	HA24	AB17	P	**HVCC**	J25	IO	MD56	N22	IO	TA5
AB05	P	**CVCC**	N10	P	**GND**	AB11	IO	HA25	AB18	P	**HVCC**	J23	IO	MD57	P25	IO	TA6
AB21	P	**CVCC**	N11	P	**GND**	AD10	IO	HA26	AB19	P	**HVCC**	K25	IO	MD58	P26	IO	TA7
AE07	IO	D/C#	N12	P	**GND**	AC10	IO	HA27	AA01	IO	IRDY#	K23	IO	MD59	P23	IO	TA8
AB02	IO	DEVSEL#	N13	P	**GND**	AC11	IO	HA28	AF09	O	KEN#	L25	IO	MD60	R26	IO	TA9
D15	O	DS0#	N14	P	**GND**	AD11	IO	HA29	T01	IO	LOCK#	L23	IO	MD61	AB03	IO	TRDY#
G22	O	DS1#	N15	P	**GND**	AB12	IO	HA30	AC09	IO	M/IO#	M25	IO	MD62	P24	O	TWE#
D16	O	DS2#	N16	P	**GND**	AE11	IO	HA31	B19	O	MA02	M23	IO	MD63	AF06	IO	W/R#
H22	O	DS3#	P11	P	**GND**	P05	I	HCLK	C19	O	MA03	D14	IO	MPD0			
AE06	O	EADS#	P12	P	**GND**	T23	IO	HD00	D19	O	MA04	B15	IO	MPD1			

Table 1. VT82C597 / VT82C597AT Pin Descriptions

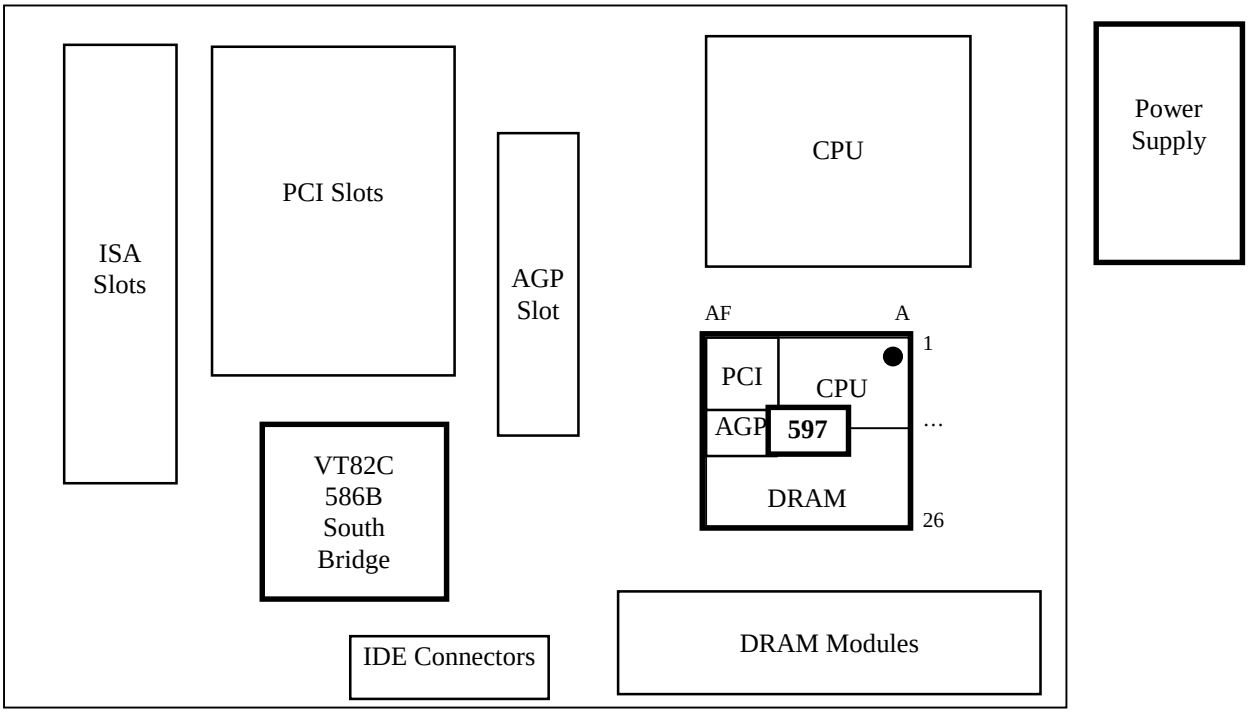
CPU Interface				
Signal Name	**597 Pin #**	**597AT Pin #**	**I/O**	**Signal Description**
ADS#	AD7	AD7	B	**Address Strobe.** The CPU asserts ADS# in T1 of the CPU bus cycle to initiate a command
M/IO#	AC9	AC9	B	**Memory / IO Command Indicator**
W/R#	AF6	AF6	B	**Write / Read Command Indicator**
D/C#	AE7	AE7	B	**Data / Control Command Indicator**
BRDY#	AC8	AC8	B	**Bus Ready.** The VT82C597 asserts BRDY# to indicate to the CPU that data is available on reads or has been received on writes.
EADS#	AE6	AE6	O	**External Address Strobe.** Asserted by the VT82C597 to inquire the L1 cache when serving PCI master accesses to main memory.
KEN# / INV	AF9	AF9	O	**Cache Enable / Invalidate.** KEN# / INV functions as both the KEN# signal during CPU read cycles and the INV signal during L1 cache snoop cycles.
HITM#	AF7	AF7	I	**Hit Modified.** Asserted by the CPU to indicate that the address presented with the last assertion of EADS# is modified in the L1 cache and needs to be written back.
HLOCK#	AF5	AF5	I	**Host Lock.** All CPU cycles sampled with the assertion of HLOCK# and ADS# until the negation of HLOCK# must be atomic.
CACHE#	AD9	AD9	I	**Cacheable Indicator.** Asserted by the CPU during a read cycle to indicate the CPU can perform a burst line fill. Asserted by the CPU during a write cycle to indicate that the CPU will perform a burst write-back cycle.
AHOLD	AE9	AE9	O	**Address Hold.** The VT82C597 asserts AHOLD when a PCI master is accessing main memory. AHOLD is held for the duration of the PCI burst transfer.
NA#	AD8	AD8	O	**Next Address Indicator.**
BOFF#	AE8	AE8	O	**Back Off.** Asserted by the VT82C597 when required to terminate a CPU cycle that was in progress.
SMIACT#	AF8	AF8	I	**System Management Interrupt Active.** This is asserted by the CPU when it is in system management mode as a result of SMI.
BE[7:0]#	AD16, AC16, AB16, AF17, AE17, AD17, AC17, AF18	AD16, AC16, AB16, AF17, AE17, AD17, AC17, AF18	B	**Byte Enables.** The CPU byte enables indicate which byte lane the current CPU cycle is accessing.
HA[31:3]	(see pinout tables)	(see pinout tables)	B	**Host Address Bus.** HA[31:3] connect to the address bus of the host CPU. During CPU cycles HA[31:3] are inputs. These signals are driven by the VT82C597 during cache snooping operations.
HD[63:0]	(see pinout tables)	(see pinout tables)	B	**Host CPU Data.** These signals are connected to the CPU data bus.

Note: Clocking of the CPU and cache interfaces is performed with HCLK; see the clock pin group at the end of the pin descriptions section for descriptions of the clock input pins.

Cache Control				
Signal Name	**597 Pin #**	**597AT Pin #**	**I/O**	**Signal Description**
CADS#	T25	T25	O	**Cache Address Strobe.** Assertion causes the burst SRAM to load the address register from address pins. Connected to all cache SRAMs.
CADV#	T24	T24	O	**Cache Advance.** Assertion causes the burst SRAM to advance to the next Quadword in the cache line. Connected to all cache SRAMs.
COE1#	R25	R25	O	**Cache Output Enable.** Typically connected to all cache SRAMs.
CCS1#	R24	R24	O	**Cache Chip Select.** Typically connected to all cache SRAMs.
TA[9:0]	R26, P23, P26, P25, N22, N23, N24, M26, N26, N25	R26, P23, P26, P25, N22, N23, N24, M26, N26, N25	B	**Tag Address.** TA0-9 are inputs during CPU accesses and outputs during L2 cache line fills and L2 line invalidates during inquire cycles.
TWE#	P24	P24	O	**Tag Write Enable.** When asserted, new state and tag addresses are written into the external tag. Connected to all cache SRAMs.
GWE#	T26	T26	O	**Global Write Enable.** Connected to all cache SRAMs.
BWE#	R23	R23	O	**Byte Write Enable.** Connected to all cache SRAMs.

Note: Only Pipeline Burst SRAMs are supported for cache.

Note: The VT82C597 pinouts were defined assuming the ATX PCB layout model shown below (and general pin layout shown) as a guide for PCB component placement. Other PCB layouts (AT, LPX, and NLX) were also considered and can typically follow the same general component placement. For PCB layouts that require different component placements from that shown below (i.e., for component placements that don't allow optimal layouts using the VT82C597), the VT82C597AT alternate pinout is available.



DRAM Interface				
Signal Name	**597 Pin #**		**I/O**	**Signal Description**
MD[63:0]	(see pinout tables)	(see pinout tables)	B	**Memory Data.** These signals are connected to the DRAM data bus. Note: MD0 is internally pulled up for use in EDO memory type detection.
MPD[7:0]	H4, L4, W4, Y4, J4, K4, W5, AA4	D23, D25, C15, A15, D24, D26, B15, D14	B	**DRAM ECC or EC Data**
MA[13:2], MAA[1:0], MAB[1:0]	N2, N1, P3, P2, P1, N4, R3, R2, R1, P4, T3, T2, M1, N3, T1, R4	A22, D21, C21, B21, A21, D20, C20, B20, A20, D19, C19, B19, C22, B22, A19, D18	O	**Memory Address.** DRAM address lines.
RAS#[5:0] / CS#[5:0]	M2, M3, L1, M4, L2, L3	D22, A23, B23, C23, A24, B24	O	**Multifunction Pins** 1. FPG/EDO DRAM: Row Address Strobe of each bank. 2. Synchronous DRAM: Chip select of each bank.
CAS#[7:0] / DQM#[7:0]	J1, V3, K2, V2, K3, T4, K1, V1	B26, B25, C17, B17, A26, A25, D17, A17	O	**Multifunction Pins** 1. FPG/EDO DRAM: Column Address Strobe of each byte lane. 2. Synchronous DRAM: Data mask of each byte lane.
SRASA#, SRASB#, SRASC#	U3, U2, U1	C18, B18, A18	O	**Row Address Command Indicator.** For support of up to three Synchronous DRAM DIMM slots (these are not copies as each DIMM slot may have separate timing). “A” controls banks 0-1 (module 0), “B” controls banks 2-3 (module 1), and “C” controls banks 4-5 (module 2).
SCASA#, SCASB#, SCASC#	W3, W2, W1	C16, B16, A16	O	**Column Address Command Indicator.** For support of up to three Synchronous DRAM DIMM slots (these are not copies as each DIMM slot may have separate timing). “A” controls banks 0-1 (module 0), “B” controls banks 2-3 (module 1), and “C” controls banks 4-5 (module 2).
SWEA# / MWEA#, SWEB# / MWEB#, SWEC# / MWEC#	J2, J3, H1	C26, C25, C24	O	**Write Enable Command Indicator.** For support of up to three Synchronous DRAM DIMM slots (these are not copies as each DIMM slot may have separate timing). Multifunction pins, used as MWE# pins for FPG/EDO memory. “A” controls banks 0-1 (module 0), “B” controls banks 2-3 (module 1), and “C” controls banks 4-5 (module 2).
DS[3:0]#	E4, V4, F4, U4	H22, D16, G22, D15	O	**SDRAM-II Data Strobes.** Every 16 data bits share one common data strobe. I.e., DS0# corresponds to MD[15:0], DS1# corresponds to MD[31:16], etc.

Note: Clocking of the memory subsystem is synchronous with the CPU clock (HCLK); see the clock pin group at the end of the pin descriptions section for descriptions of the clock input pins.

PCI Bus Interface				
Signal Name	**597 Pin #**	**597AT Pin #**	**I/O**	**Signal Description**
FRAME#	L25	AA2	B	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
AD[31:0]	(see pinout tables)	(see pinout tables)	B	**Address/Data Bus.** The standard PCI address and data lines. The address is driven with FRAME# assertion and data is driven or received in following cycles.
CBE[3:0]#	B26, C23, J25, K23	W4, AA3, AC1, AF2	B	**Command/Byte Enable.** Commands are driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
IRDY#	K26	AA1	B	**Initiator Ready.** Asserted when the initiator is ready for data transfer.
TRDY#	K25	AB3	B	**Target Ready.** Asserted when the target is ready for data transfer.
STOP#	A22	AB1	B	**Stop.** Asserted by the target to request the master to stop the current transaction.
DEVSEL#	J26	AB2	B	**Device Select.** This signal is driven by the VT82C597 when a PCI initiator is attempting to access main memory. It is an input when the VT82C597 is acting as a PCI initiator.
PAR	D20	AC2	B	**Parity.** A single parity bit is provided over AD[31:0] and C/BE[3:0].
SERR#	C22	AB4	B	**System Error.** VT82C597 will pulse this signal when it detects a system error condition.
LOCK#	B22	T1	B	**Lock.** Used to establish, maintain, and release resource lock.
PREQ#	M24	AC6	I	**PCI Request.** This signal comes from the South Bridge. PREQ# is the South Bridge request for the PCI bus.
PGNT#	L26	AD6	O	**PCI Grant.** This signal driven by the VT82C597 to grant PCI access to the South Bridge.
REQ[3:0]#	H24, G25, F26, F24	R4, R2, T4, T2	I	**Request.** PCI master requests for PCI.
GNT[3:0]#	H25, G26, G24, F25	P4, R3, R1, T3	O	**Grant.** Permission is given to the master to use PCI.

Note: Clocking of the PCI interface is performed with PCLK; see the clock pin group at the end of the pin descriptions section for descriptions of the clock input pins.

AGP Bus Interface				
Signal Name	**597 Pin #**	**597AT Pin #**	**I/O**	**Signal Description**
GFRM#	B12	J3	B	**Frame (PCI transactions only).** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
GDS0#	B8	M4	B	**Bus Strobe 0 (AGP transactions only).** Provides timing for 2x data transfer mode on AD[15:0]. The agent that is providing the data drives this signal.
GDS1#	D14	E3	B	**Bus Strobe 1 (AGP transactions only).** Provides timing for 2x data transfer mode on AD[31:16]. The agent that is providing the data drives this signal.
GD[31:0]	(see pinout tables)	(see pinout tables)	B	**Address/Data Bus.** The standard AGP/PCI address and data lines. The address is driven with GDS0# and GDS1# assertion for AGP transfers and is driven with GFRM# assertion for PCI transfers.
GBE[3:0]#	B14, D11, A10, A8	F1, G3, J4, M3	B	**Command/Byte Enable.** **AGP:** These pins provide command information (different commands than for PCI) driven by the master (graphics controller) when requests are being enqueued using PIPE#. These pins provide valid byte information during AGP write transactions and are driven by the master. The target (this chip) drives these lines to "0000" during the return of AGP read data, but the state of these pins is ignored by the AGP master. **PCI:** Commands are driven with GFRM# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
GIRDY#	C12	J2	B	**Initiator Ready** **AGP:** For write operations, the assertion of this pin indicates that the master is ready to provide *all* write data for the current transaction. Once this pin is asserted, the master is not allowed to insert wait states. For read operations, the assertion of this pin indicates that the master is ready to transfer a subsequent block of read data. The master is *never* allowed to insert a wait state during the initial block of a read transaction. However, it may insert wait states after each block transfers. **PCI:** Asserted when the initiator is ready for data transfer.
GTRDY#	A11	J1	B	**Target Ready:** **AGP:** Indicates that the target is ready to provide read data for the entire transaction (when the transaction can complete within four clocks) or is ready to transfer a (initial or subsequent) block of data when the transfer requires more than four clocks to complete. The target is allowed to insert wait states after each block transfers on both read and write transactions. **PCI:** Asserted when the target is ready for data transfer.
GSTOP#	C11	K3	B	**Stop (PCI transactions only).** Asserted by the target to request the master to stop the current transaction.
GDSEL#	B11	H4	B	**Device Select (PCI transactions only).** This signal is driven by the VT82C597 when a PCI initiator is attempting to access main memory. It is an input when the VT82C597 is acting as PCI initiator. Not used for AGP cycles.

Note: Clocking of the AGP interface is performed with GCLK; see the clock pin group for descriptions of the clock input pins.

Note: PCB Layout Guidelines (reference from AGP specification)

1. Total motherboard trace length 10” max, trace impedance = 65 ohms ± 15 ohms, minimize signal crosstalk
2. Trace lengths within groups matched to within 2 inches or better
   Groups are:
   a. GDS0#, GD15-0, GBE1-0#
   b. GDS1#, GD31-16, GBE3-2#
   c. SBS#, SBA7-0
3. Ground isolation should be provided around GDS0# and GDS1# to prevent crosstalk with GD[31:0]. Ideally ground traces should be provided adjacent to GDSn# on the same signal layer, but at a minimum wider spaces should be provided on either side (e.g., 16 mil spaces on either side of GDSn# if GDSn# signal traces are 8 mil).

AGP Bus Interface (continued)				
Signal Name	**597 Pin #**	**597AT Pin #**	**I/O**	**Signal Description**
GPIPE#	B19	A3	I	**Pipelined Request (AGP only).** Asserted by the master (graphics controller) to indicate that a full-width request is to be enqueued by the target (VT82C597). The master enqueues one request each rising edge of GCLK while PIPE# is asserted. When PIPE# is deasserted no new requests are enqueued across the AD bus.
GRBF#	C19	B3	I	**Read Buffer Full (AGP only).** Indicates if the master (graphics controller) is ready to accept previously requested low priority read data or not. When RBF# is asserted, the VT82C597 will not return low priority read data to the master.
SBA[7:0]	C17, D16, A17, B17, B18, D17, A18, D18	C2, B1, A1, D5, A2, C5, C3, A6	I	**SideBand Address (AGP only).** Provides an additional bus to pass address and command information from the master (graphics controller) to the target (the VT82C597). These pins are ignored until enabled.
SBS#	C18	B2	I	**Sideband Strobe (AGP only).** Provides timing for SBA[7:0] and is driven by the master.
ST[2:0]	D21, B20, A19	E8, B4, C4	O	**Status (AGP only).** Provides information from the arbiter to a master to indicate what it may do. Only valid while GGNT# is asserted. 000 Indicates that previously requested low priority read or flush data is being returned to the master (graphics controller). 001 Indicates that previously requested high priority read data is being returned to the master. 010 Indicates that the master is to provide low priority write data for a previously enqueued write command. 011 Indicates that the master is to provide high priority write data for a previously enqueued write command. 100 Reserved. (Arbiter must not issue. May be defined in the future). 101 Reserved. (Arbiter must not issue. May be defined in the future). 110 Reserved. (Arbiter must not issue. May be defined in the future). 111 Indicates that the master (graphics controller) has been given permission to start a bus transaction. The master may enqueue AGP requests by asserting PIPE# or start a PCI transaction by asserting GFRM#. ST[2:0] are always outputs from the VT82C597 and inputs to the master.
GREQ#	A20	A4	I	**Request.** Master request for AGP.
GGNT#	B21	B5	O	**Grant.** Permission is given to the master to use AGP.
GPAR	A21	B6	B	**Parity.** A single parity bit is provided over GD[31:0] and GBE[3:0].
GSERR#	C20	A5	B	**System Error.** VT82C597 will pulse this signal when it detects a system error condition.
-reserved-	C21	C6	-	**Reserved.** Do not connect. Reserved for future use.
-reserved-	E20	D6	-	**Reserved.** Do not connect. Reserved for future use.

Note: For PCI operation on the AGP bus, the following pins are not required:
- PERR# (parity and error reporting not required on transient data devices such as graphics controllers)
- LOCK# (no lock requirement on AGP)
- IDSEL (internally connected to AD16 on AGP-compliant masters)

Note: Separate system interrupts are not provided for AGP. The AGP connector provides interrupts via PCI bus INTA-B#.

Note: The AGP bus supports only one master directly (REQ[3:0]# and GNT[3:0]# are not provided). External logic is required to implement additional master capability. Note that the arbitration mechanism on the AGP bus is different from the PCI bus.

Note: A separate reset is not required for the AGP bus (RESET# resets both PCI and AGP buses)

Note: Two mechanisms are provided by the AGP bus to enqueue master requests: PIPE# (to send addresses multiplexed on the AD lines) and the SBA port (to send addresses unmultiplexed). AGP masters implement one or the other or select one at initialization time (they are not allowed to change during runtime). Therefore only one of the two will be used and the signals associated with the other will not be used. Therefore the 82C597 has an internal pullup on RBF# to maintain it in the de-asserted state in case it is not implemented on the master device.

Clock / Reset Control				
Signal Name	**597 Pin #**	**597AT Pin #**	**I/O**	**Signal Description**
HCLK	N5	P5	I	**Host Clock.** This pin receives a buffered host clock. This clock is used by all of the VT82C597 logic that is in the host CPU and memory clock domains. This should be the same clock net that is delivered to the CPU.
GCLK / **GND**	E8	D4	I	**AGP Clock.** This pin is provided for test purposes and should be connected to ground.
PCLK	D19	W5	I	**PCI Clock.** This pin receives a buffered divided-by-2 host clock. This clock is used by all of the VT82C597 logic that is in the PCI clock domain. This clock input must be 33 MHz maximum to comply with PCI specification requirements and must be synchronous with HCLK with an HCLK:PCLK frequency ratio of 2:1. Typical Clock Frequency Combinations Mode / Host Clock / AGP Clock / PCI Clock 2x / 60 MHz / 60 MHz / 30 MHz 2x / 66 MHz / 66 MHz / 33 MHz
RESET#	M25	AC7	I	**Reset.** When asserted, this signal resets the VT82C597 and sets all register bits to the default value. This signal also connects to the PCI bus, to the AGP bus, and (through an inverter) to the ISA bus (if implemented).

Power and Ground				
Signal Name	**597 Pin #**	**597AT Pin #**	**I/O**	**Signal Description**
CVCC	E5, F22, AB5, AB21	E5, F22, AB5, AB21	P	**Power** for **internal logic** (3.3V ±5%).
HVCC	U22, V22, AB9, AB10, AB17, AB18, AB19	U22, V22, AB9, AB10, AB17, AB18, AB19	P	**Power** for **CPU interface** (2.5V to 3.3V ±5%).
MVCC	G5, H5, J5, R5, T5, U5, V5, AB6, AB7	E9, E10, E11, E17, E18, E19, J22, K22, L22	P	**Power** for **Memory interface** (3.3V ±5%).
PVCC	J22, K22, L22	R5, T5, U5, V5, AB6, AB7	P	**Power** for **PCI interface** (3.3V ±5%).
GVCC	E9, E10, E11, E17, E18, E19	G5, H5, J5	P	**Power** for **AGP interface** (3.3V ±5%).
AVCC	F5	K5	P	**Analog Power** (3.3V ±5%). For internal clock logic.
AGND	K5	N5	P	**Analog Ground.** For internal clock logic. Connect to main ground plane.
GND	D8, E6-E7, E14-E16, E22, J9, J14, J18, K10, K14, K17, L5, L11-L16, M5, M11-M16, N9-N16, P11-P18, P22, R11-R16, R22, T11-T16, U10, U13, U17, V9, V13, V18, Y5, AA5, AA22, AB13, AB14, AB22	D8, E6-E7, E14-E16, E22, J9, J14, J18, K10, K14, K17, L5, L11-L16, M5, M11-M16, N9-N16, P11-P18, P22, R11-R16, R22, T11-T16, U10, U13, U17, V9, V13, V18, Y5, AA5, AA22, AB13, AB14, AB22	P	**Ground**
5VREF	E21, AB8	E21, AB8	P	**5V Reference** (5V ±5%). Used to provide 5V input tolerance.
GVREF	E13	F5	P	**AGP Voltage Reference.** 0.39 GVCC to 0.41 GVCC. Typical value is 1.32V (0.40 times 3.3V). This can be provided with a resistive divider on GVCC using 270 ohm and 180 ohm (2%) resistors.
MVREF	P5	E20	P	**DRAM Voltage Reference.** 1.5V for SDRAM, 1.0V for SDRAM-II (±5%)

REGISTERS

Register Overview

The following tables summarize the configuration and I/O registers of the VT82C597. These tables also document the power-on default value ("Default") and access type ("Acc") for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), "—" for reserved / used (essentially the same as RO), and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions for details).

Detailed register descriptions are provided in the following section of this document. All offset and default values are shown in hexadecimal unless otherwise indicated.

Table 2. VT82C597 Registers

VT82C597 Device 0 Registers - Host Bridge

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	0597	RO
5-4	Command	0006	**RW**
7-6	Status	0290	**WC**
8	Revision ID	nn	RO
9	Program Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	06	RO
C	-reserved- (cache line size)	00	—
D	Latency Timer	00	**RW**
E	Header Type	00	RO
F	Built In Self Test (BIST)	00	RO
13-10	Graphics Aperture Base	0000 0008	RW
14-27	-reserved- (base address registers)	00	—
28-2F	-reserved- (unassigned)	00	—
33-30	-reserved- (expan ROM base addr)	00	—
37-34	Capability Pointer	0000 00A0	RO
34-3B	-reserved- (unassigned)	00	—
3C-3D	-reserved- (interrupt line & pin)	00	—
3E-3F	-reserved- (min gnt and max latency)	00	—

Device-Specific Registers

Offset	Cache Control	Default	Acc
50	Cache Control 1	00	RW
51	Cache Control 2	00	RW
52	Non-Cacheable Control	00	RW
53	System Performance Control	00	RW
55-54	Non-Cacheable Region #1	0000	RW
57-56	Non-Cacheable Region #2	0000	RW

Offset	DRAM Control	Default	Acc
59-58	MA Map Type	0000	RW
5A-5F	DRAM Row Ending Address:		
5A	Bank 0 Ending (HA[29:22])	01	RW
5B	Bank 1 Ending (HA[29:22])	01	RW
5C	Bank 2 Ending (HA[29:22])	01	RW
5D	Bank 3 Ending (HA[29:22])	01	RW
5E	Bank 4 Ending (HA[29:22])	01	RW
5F	Bank 5 Ending (HA[29:22])	01	RW
60	DRAM Type	00	RW
61	ROM Shadow Control C0000-CFFFF	00	RW
62	ROM Shadow Control D0000-DFFFF	00	RW
63	ROM Shadow Control E0000-FFFFF	00	RW
64	DRAM Timing for Banks 0,1	EC	RW
65	DRAM Timing for Banks 2,3	EC	RW
66	DRAM Timing for Banks 4,5	EC	RW
67	-reserved- (unassigned)	00	RW
68	DRAM Control	00	RW
69	-reserved- (unassigned)	00	RW
6A	DRAM Refresh Counter	00	RW
6B	DRAM Arbitration Control	01	RW
6C	SDRAM Control	00	RW
6D	DRAM Control Drive Strength	00	RW
6E	ECC Control	00	RW
6F	ECC Status	00	**RO**

Offset	PCI Bus Control	Default	Acc
70	PCI Buffer Control	00	RW
71	CPU to PCI Flow Control 1	00	RW
72	CPU to PCI Flow Control 2	00	RW
73	PCI Master Control 1	00	RW
74	PCI Master Control 2	00	RW
75	PCI Arbitration 1	00	RW
76	PCI Arbitration 2	00	RW
77	Chip Test (do not program)	00	RW
78-7D	-reserved-	00	—
7E	DLL Test Mode (do not program)	00	RW
7F	DLL4 Test Mode (do not program)	00	RW
80-FF	-reserved-	00	—

Offset	GART/TLB Control	Default	Acc
83-80	GART/TLB Control	0000 0000	RW
84	Graphics Aperture Size	00	RW
85-87	-reserved- (unassigned)	00	—
8B-88	Gr. Aperture Translation Table Base	0000 0000	RW
8C-8F	-reserved- (unassigned)	00	—

Offset	AGP Control	Default	Acc
A0	AGP ID	02	RO
A1	AGP Next Item Pointer	00	RO
A2	AGP Specification Revision	10	RO
A3	-reserved- (unassigned)	00	—
A7-A4	AGP Status	0700 0203	RO
AB-A8	AGP Command	0000 0000	**RW**
AC-AE	-reserved- (unassigned)	00	—
AF	AGP Control	00	RW

VT82C597 Device 1 - PCI-to-PCI Bridge

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	8597	RO
5-4	Command	0007	**RW**
7-6	Status	0220	**WC**
8	Revision ID	nn	RO
9	Program Interface	00	RO
A	Sub Class Code	04	RO
B	Base Class Code	06	RO
C	-reserved- (cache line size)	00	—
D	Latency Timer	00	**RW**
E	Header Type	01	RO
F	Built In Self Test (BIST)	00	RO
10-17	-reserved- (base address registers)	00	—
18	Primary Bus Number	00	**RW**
19	Secondary Bus Number	00	**RW**
1A	Subordinate Bus Number	00	**RW**
1B	-reserved- (secondary latency timer)	00	—
1C	I/O Base	F0	**RW**
1D	I/O Limit	00	**RW**
1F-1E	Secondary Status	0000	RO
21-20	Memory Base	FFF0	**RW**
23-22	Memory Limit (Inclusive)	0000	**RW**
25-24	Prefetchable Memory Base	FFF0	**RW**
27-26	Prefetchable Memory Limit	0000	**RW**
28-3D	-reserved- (unassigned)	00	—
3F-3E	PCI-to-PCI Bridge Control	00	RW

Device-Specific Registers

Offset	PCI Bus #2 Control	Default	Acc
40	CPU-to-PCI Flow Control 1	00	RW
41	CPU-to-PCI Flow Control 2	00	RW
42	PCI Master Control	00	RW
43-4F	-reserved- (unassigned)	00	—

Configuration Space I/O

All registers in the VT82C597 (listed above) are addressed via the following configuration mechanism:

Mechanism #1

These ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

Port CFB-CF8 - Configuration Address..... RW

31 Configuration Space Enable
- 0 Disabled..... default
- 1 Convert configuration data port writes to configuration cycles on the PCI bus

30-24 Reserved .....always reads 0

23-16 PCI Bus Number
Used to choose a specific PCI bus in the system

15-11 Device Number
Used to choose a specific device in the system (devices 0 and 1 are defined for the VT82C597)

10-8 Function Number
Used to choose a specific function if the selected device supports multiple functions (only function 0 is defined for the VT82C597).

7-2 Register Number (also called the "Offset")
Used to select a specific DWORD in the VT82C597 configuration space

1-0 Fixed .....always reads 0

Port CFF-CFC - Configuration Data..... RW

Refer to PCI Bus Specification Version 2.1 for further details on operation of the above configuration registers.

Register Descriptions

Device 0 Header Registers - Host Bridge

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number, function number, and device number equal to zero.

Device 0 Offset 1-0 - Vendor ID ..... RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 0 Offset 3-2 - Device ID ..... RO

15-0 ID Code (reads 0597h to identify the VT82C597)

Device 0 Offset 5-4 - Command ..... RW

15-10 Reserved ..... always reads 0

9 Fast Back-to-Back Cycle Enable ..... RW
- 0 Fast back-to-back transactions only allowed to the same agent ..... default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable ..... RO
- 0 SERR# driver disabled ..... default
- 1 SERR# driver enabled

(SERR# is used to report parity errors if bit-6 is set).

7 Address / Data Stepping ..... RO
- 0 Device never does stepping ..... default
- 1 Device always does stepping

6 Parity Error Response ..... RW
- 0 Ignore parity errors & continue ..... default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop ..... RO
- 0 Treat palette accesses normally ..... default
- 1 Don't respond to palette accesses on PCI bus

4 Memory Write and Invalidate Command ..... RO
- 0 Bus masters must use Mem Write ..... default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring ..... RO
- 0 Does not monitor special cycles ..... default
- 1 Monitors special cycles

2 Bus Master ..... RO
- 0 Never behaves as a bus master
- 1 Can behave as a bus master ..... default

1 Memory Space ..... RO
- 0 Does not respond to memory space
- 1 Responds to memory space ..... default

0 I/O Space ..... RO
- 0 Does not respond to I/O space ..... default
- 1 Responds to I/O space

Device 0 Offset 7-6 - Status ..... RWC

15 Detected Parity Error
- 0 No parity error detected ..... default
- 1 Error detected in either address or data phase. This bit is set even if error response is disabled (command register bit-6). .....write one to clear

14 Signaled System Error (SERR# Asserted) ..... always reads 0

13 Signaled Master Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the master ..... write one to clear

12 Received Target Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the target..... write 1 to clear

11 Signaled Target Abort ..... always reads 0
- 0 Target Abort never signaled

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium ..... always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected
- 0 No data parity error detected ..... default
- 1 Error detected in data phase. Set only if error response enabled via command bit-6 = 1 and VT82C597 was initiator of the operation in which the error occurred. .....write one to clear

7 Fast Back-to-Back Capable ..... always reads 1

6 Reserved ..... always reads 0

5 66MHz Capable ..... always reads 0

4 Supports New Capability list ..... always reads 1

3-0 Reserved ..... always reads 0

Device 0 Offset 8 - Revision ID ..... RO

7-0 VT82C597 Chip Revision Code
- 00 First Silicon (Revision "A")
- 01 Production Silicon (Revision "B")

Device 0 Offset 9 - Programming Interface ..... RO

7-0 Interface Identifier ..... always reads 00

Device 0 Offset A - Sub Class Code ..... RO

7-0 Sub Class Code ..... reads 00 to indicate Host Bridge

Device 0 Offset B - Base Class Code ..... RO

7-0 Base Class Code .. reads 06 to indicate Bridge Device

Device 0 Offset D - Latency Timer ..... RW

Specifies the latency timer value in PCI bus clocks.

7-3 Guaranteed Time Slice for CPU ..... default=0

2-0 Reserved (fixed granularity of 8 clks) . always reads 0

Bits 2-1 are writeable but read 0 for PCI specification compatibility. The programmed value may be read back in Offset 75 bits 5-4 (PCI Arbitration 1).

Device 0 Host Bridge Header Registers (continued)

Device 0 Offset E - Header Type.....RO

7-0 Header Type Code .....reads 00: single function

Device 0 Offset F - Built In Self Test (BIST).....RO

7 BIST Supported .....reads 0: no supported functions
6 Start Test .....write 1 to start but writes ignored
5-4 Reserved ..... always reads 0
3-0 Response Code..... 0 = test completed successfully

Device 0 Offset 13-10 - Graphics Aperture Base .....RW

31-28 Upper Programmable Base Address Bits..... def=0
27-20 Lower Programmable Base Address Bits ..... def=0
These bits behave as if hardwired to 0 if the corresponding Graphics Aperture Size register bit (Device 1 Offset 84h) is 0.

27	26	25	24	23	22	21	20	(This Register)
7	6	5	4	3	2	1	0	(Gr Aper Size)
RW	RW	RW	RW	RW	RW	RW	RW	1M
RW	RW	RW	RW	RW	RW	RW	0	2M
RW	RW	RW	RW	RW	RW	0	0	4M
RW	RW	RW	RW	RW	0	0	0	8M
RW	RW	RW	RW	0	0	0	0	16M
RW	RW	RW	0	0	0	0	0	32M
RW	RW	0	0	0	0	0	0	64M
RW	0	0	0	0	0	0	0	128M
0	0	0	0	0	0	0	0	256M

19-0 Reserved ..... always reads 00008

Note: The locations in the address range defined by this register are prefetchable.

Device 0 Offset 37-34 - Capability Pointer.....RO

Contains an offset from the start of configuration space.

31-0 AGP Capability List Pointer.....always reads A0h

Device 0 Configuration Registers - Host Bridge

This group of registers is pointed to by the value in offset 34.

Cache Control

Device 0 Offset 50 - Cache Control 1.....RW

7-6 Cache Enable / Initialize
- 00 Cache disable .....default
- 01 Cache Initialize - always does L2 fill
- 10 Cache enable (normal operation)
- 11 Reserved (do not use)

5 Linear Burst
- 0 Disable .....default
- 1 Enable

4-3 Tag Configuration
- 00 8+0 - 8 Tag bits, no alt (dirty) bit.....default
- 01 7+1 - 7 Tag bits + alternate (dirty) bit
- 10 10+0 - 10 Tag bits, no alternate (dirty) bit
- 11 9+1 - 9 Tag bits + alternate (dirty) bit

2-0 Reserved .....always read 0

Device 0 Offset 51 - Cache Control 2.....RW

7-6 Reserved (no function)..... RW

5 Backoff CPU

Set to one to backoff CPU when non-streaming access to fill L2 cache. Used when register 52h bit-2 is set for "L2 fill when CACHE# is inactive". This bit should normally be set to 0 for best performance, but performance differences are typically not significantly noticeable at the system level.
- 0 Defer ready return until L2 is filled.....default
- 1 Backoff CPU until L2 is filled

4 Reserved ..... always reads 0

3 SRAM Banks.....(default set from inverse of HA29)
- 0 1 Bank
- 1 2 Banks

2 Reserved ..... always reads 0

1-0 Cache Size (bit-0 default set from inverse of HA31)
- 00 256K
- 01 512K
- 10 1M
- 11 2M

Table 3. COAST Module Detection

Pins HA28-31 have internal pull-ups (external pull-downs may be used to change the default value read on reset) and TA8 has an internal pull-down (an external pull-up may be used to change the default value). The bits affected are:

Rx51[0] = Cache Size bit-0 = not HA31
Rx51[1] = Cache Size bit-1 = reset to 0 (no 1M/2M detect)

Rx51[3] = SRAM Banks = not HA29 (inverted HA29)

Device 0 Offset 52 - Non-Cacheable Control RW

7 **C0000-C7FFF Cacheable & Write-Protect** ... def=0
6 **D0000-DFFFF Cacheable & Write-Protect** ... def=0
5 **E0000-EFFFF Cacheable & Write-Protect** ... def=0
4 **F0000-FFFFF Cacheable & Write-Protect** .... def=0
3 **Reserved** ..... always reads 0
2 **L2 Fill on Single Read**
0 Normal L2 cache fill.....default
1 Force the requested data to be filled into the L2 cache (provided that L2 cache is enabled), even if the CPU does a read cycle with CACHE# de-asserted. Setting this bit significantly improves performance.
1 **Reserved** ..... always reads 0
0 **L2 Write Thru/Write-Back**
0 Write-Back .....default
1 Write-Thru

Device 0 Offset 53 - System Performance Control .....RW

7 **Read Around Write**
0 Disable .....default
1 Enable
6 **Cache Read Pipeline Cycle**
0 Disable .....default
1 Enable
5 **Cache Write Pipeline Cycle**
0 Disable .....default
1 Enable
4 **DRAM Read Pipeline Cycle**
0 Disable .....default
1 Enable
3-0 **Reserved** ..... always reads 0

Device 0 Offset 55-54 - Non-Cacheable Region #1..... RW

15-3 **Base Address** - A<28:16> .....default=0
As noted below, the base address must be a multiple of the region size.
2-0 **Range (Region Size)**
000 Disable..... default
001 64K
010 128K (Base Address A16 must be 0)
011 256K (Base Address A16-17 must be 0)
100 512K (Base Address A16-18 must be 0)
101 1M (Base Address A16-19 must be 0)
110 2M (Base Address A16-20 must be 0)
111 4M (Base Address A16-21 must be 0)

Device 0 Offset 57-56 - Non-Cacheable Region #2..... RW

15-3 **Base Address MSBs** - A<28:16> .....default=0
As noted below, the base address must be a multiple of the region size.
2-0 **Range (Region Size)**
000 Disable..... default
001 64K
010 128K (Base Address A16 must be 0)
011 256K (Base Address A16-17 must be 0)
100 512K (Base Address A16-18 must be 0)
101 1M (Base Address A16-19 must be 0)
110 2M (Base Address A16-20 must be 0)
111 4M (Base Address A16-21 must be 0)

DRAM Control

These registers are normally set at system initialization time and not accessed after that during normal system operation. Some of these registers, however, may need to be programmed using specific sequences during power-up initialization to properly detect the type and size of installed memory (refer to the VIA Technologies 82C597 BIOS porting guide for details).

Table 4. System Memory Map

Space	Start	Size	Address Range	Comment
DOS	0	640K	00000000-0009FFFF	Cacheable
VGA	640K	128K	000A0000-000BFFFF	Used for SMM
BIOS	768K	16K	000C0000-000C3FFF	Shadow Ctrl 1
BIOS	784K	16K	000C4000-000C7FFF	Shadow Ctrl 1
BIOS	800K	16K	000C8000-000CBFFF	Shadow Ctrl 1
BIOS	816K	16K	000CC000-000CFFFF	Shadow Ctrl 1
BIOS	832K	16K	000D0000-000D3FFF	Shadow Ctrl 2
BIOS	848K	16K	000D4000-000D7FFF	Shadow Ctrl 2
BIOS	864K	16K	000D8000-000DBFFF	Shadow Ctrl 2
BIOS	880K	16K	000DC000-000DFFFF	Shadow Ctrl 2
BIOS	896K	64K	000E0000-000EFFFF	Shadow Ctrl 3
BIOS	960K	64K	000F0000-000FFFFF	Shadow Ctrl 3
Sys Bus Init	1MB D Top 4G-64K	— 64K	00100000-DRAM Top DRAM Top-FFFEFFFF FFFEFFFF-FFFFFFFF	Can have hole 000Fxxxx alias

Device 0 Offset 59-58 - DRAM MA Map Type.....RW

15-13 Bank 5/4 MA Map Type (EDO/FPG)
- 000 8-bit Column Address
- 001 9-bit Column Address
- 010 10-bit Column Address .....default
- 011 11-bit Column Address
- 100 12-bit Column Address (64Mb)
- 101 Reserved
- 11x Reserved

Bank 5/4 MA Map Type (SDRAM)
- 0xx 16Mbit SDRAM.....default
- 1xx 64Mbit SDRAM

12-8 Reserved ..... always reads 0

7-5 Bank 1/0 MA Map Type (see above)

4 Reserved ..... always reads 0

3-1 Bank 3/2 MA Map Type (see above)

0 Reserved ..... always reads 0

Device 0 Offset 5A-5F - DRAM Row Ending Address:

All of the registers in this group default to 01h:

Offset 5A - Bank 0 Ending (HA[30:23]) ..... RW

Offset 5B - Bank 1 Ending (HA[30:23]).....RW

Offset 5C - Bank 2 Ending (HA[30:23]) ..... RW

Offset 5D - Bank 3 Ending (HA[30:23]) ..... RW

Offset 5E - Bank 4 Ending (HA[30:23]).....RW

Offset 5F - Bank 5 Ending (HA[30:23]).....RW

Note :BIOS is required to fill the ending address registers for all banks even if no memory is populated. The endings have to be in incremental order.

Device 0 Offset 60 - DRAM Type ..... RW

7-6 Reserved .....always reads 0

5-4 DRAM Type for Bank 5/4
- 00 Fast Page Mode DRAM (FPG)..... default
- 01 EDO DRAM (EDO)
- 10 SDRAM Double Data Rate (DDR SDRAM-II)
- 11 SDRAM Single Data Rate (SDR SDRAM)

3-2 DRAM Type for Bank 3/2.....default=FPG

1-0 DRAM Type for Bank 1/0.....default=FPG

Table 5. Memory Address Mapping Table

EDO/FP DRAM

MA:	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
8-bit Col (000)		**23**	22	21	11	20	19 10	18 9	17 8	16 7	15 6	14 5	13 4	12 3	Row Bits Col Bits
9-bit Col (001)		**24**	**23**	**22**	21	20 11	19 10	18 9	17 8	16 7	15 6	14 5	13 4	12 3	Row Bits Col Bits
10-bit Col (010)		**25**	**24**	23	21 22	20 11	19 10	18 9	17 8	16 7	15 6	14 5	13 4	12 3	Row Bits Col Bits
11-bit Col (011)		**26**	25	23 24	21 22	20 11	19 10	18 9	17 8	16 7	15 6	14 5	13 4	12 3	Row Bits Col Bits
12-bit Col (100)		27	25 26	23 24	21 22	20 11	19 10	18 9	17 8	16 7	15 6	14 5	13 4	12 3	Row Bits Col Bits

SDRAM

MA:	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
16Mb (0xx)			**11** *11*	22 PC	21 24	20 23	19 10	18 9	17 8	16 7	15 6	14 5	13 4	12 3	Row Bits Col Bits
64Mb (1xx) (Rev A)	**25** ***25***	13 *13*	12 *12*	22 PC	21 26	20 **11**	19 10	18 9	17 8	16 7	15 6	14 5	**24** 4	23 3	x4: 10 col x8: 9 col
64Mb (1xx) (Rev B Production Silicon)	**24** ***24***	13 *13*	12 *12*	22 PC	21 26	20 **25**	19 10	18 9	17 8	16 7	15 6	14 5	**11** 4	23 3	x4: 10 col x8: 9 col x16: 8 col x32: 8 col

"PC" = "Precharge Control" (refer to SDRAM specifications)

16Mb 11x10, 11x9, and 11x8 configurations supported

64Mb
- x4: 12x10 4bank, 13x10 2bank supported
- x8: 12x9 4bank, 13x9 2bank supported
- x16: 12x8 4bank, 13x8 2bank supported
- x32: 11x8 4bank, 2bank (2Mx32) not supported

Device 0 Offset 61 - Shadow RAM Control 1 .....RW

7-6 CC000h-CFFFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 C8000h-CBFFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 C4000h-C7FFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

1-0 C0000h-C3FFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

Device 0 Offset 62 - Shadow RAM Control 2 .....RW

7-6 DC000h-DFFFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 D8000h-DBFFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 D4000h-D7FFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

1-0 D0000h-D3FFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

Device 0 Offset 63 - Shadow RAM Control 3..... RW

7-6 E0000h-EFFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 F0000h-FFFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 Memory Hole
- 00 None ..... default
- 01 512K-640K
- 10 15M-16M (1M)
- 11 14M-16M (2M)

1-0 SMI Mapping Control
- 00 Disable SMI Address Redirection ..... default
- 01 Allow access to DRAM Axxxx-Bxxxx
- 10 SMI 3xxxx-4xxxx redirect to Axxxx-Bxxxx (30000-4FFFFh is automatically set to noncachable)
- 11 Allow SMI Axxxx-Bxxxx DRAM access

Note: The A0000-BFFFF address range is reserved for use by VGA controllers for system access to the VGA frame buffer. Since frame buffer accesses are normally directed to the system VGA controller (with its separate memory subsystem), system DRAM locations in the A0000-BFFFF range would normally be unused. Setting the above bits appropriately allows this block of system memory to be used by directing Axxxx-Bxxxx accesses (in System Management Mode) to corresponding memory addresses in system DRAM instead of directing those accesses to the PCI bus for VGA frame buffer access.

Device 0 Offset 64 - DRAM Timing for Banks 0,1 .....RW

Device 0 Offset 65 - DRAM Timing for Banks 2,3 .....RW

Device 0 Offset 66 - DRAM Timing for Banks 4,5 .....RW

FPG / EDO Settings for Registers 64-66

7 RAS Precharge Time
- 0 3T
- 1 4T .....default

6 RAS Pulse Width
- 0 4T
- 1 5T .....default

5-4 CAS Read Pulse Width
- 00 1T
- 01 2T
- 10 3T .....default
- 11 4T

Note: EDO will not automatically reduce the CAS pulse width. For EDO type DRAMs, use 00 if CAS width = 1 is to be used.

3 CAS Write Pulse Width
- 0 1T
- 1 2T .....default

2 MA-to-CAS Delay
- 0 1T
- 1 2T .....default

1 RAS to MA Delay
- 0 1T .....default
- 1 2T

0 Reserved ..... always reads 0

SDRAM Settings for Registers 64-66

7 Precharge Command to Active Command Period
- 0 TRP = 2T
- 1 TRP = 3T ..... default

6 Active Command to Precharge Command Period
- 0 TRAS = 5T
- 1 TRAS = 6T ..... default

5-4 CAS Latency

	SDRAM	SDRAM-II	
00	1T	n/a	
01	2T	n/a	
10	3T	2T, 2.5T	..... default
11	n/a	3T	

3 DDR Write Enable (SDRAM-II Only)
- 0 Disable..... default
- 1 Enable

2 ACTIVE Command to CMD Command Period
- 0 2T
- 1 3T ..... default

1-0 Bank Interleave
- 00 No Interleave ..... default
- 01 2-way
- 10 4-way
- 11 Reserved

Device 0 Offset 68 - DRAM Control.....RW

7 SDRAM Open Page Control
- 0 Always precharge SDRAM banks when accessing EDO/FPG DRAMs.....default
- 1 SDRAM banks remain active when accessing EDO/FPG banks †

6 Bank Page Control
- 0 Allow only pages of the same bank active... def
- 1 Allow pages of different banks to be active †

5 EDO Pipeline Burst Rate
- 0 X-2-2-2-**2**-2-2-2.....default
- 1 X-2-2-2-**3**-2-2-2

4 DRAM Data Latch Delay (EDO/FPG only)
- 0 Latch DRAM data at CCLK rising edge ..... def
- 1 Delay latch of DRAM data by ½ clock

3 EDO Test Mode
- 0 Disable .....default
- 1 Enable

2 Burst Refresh
- 0 Disable .....default
- 1 Enable (burst 4 times)

1 MCACHE Enable ..... default set from TA8 pin
- 0 Disable
- 1 Enable

0 Reserved ..... always reads 0

Note: MD0 is internally pulled up for EDO detection.

Device 0 Offset 6A - Refresh Counter .....RW

7-0 Refresh Counter (in units of 16 CPUCLKs)
- 00 DRAM Refresh Disabled .....default
- 01 32 CPUCLKs
- 02 48 CPUCLKs
- 03 64 CPUCLKs
- 04 80 CPUCLKs
- 05 96 CPUCLKs
- … …

The programmed value is the desired number of 16-CPUCLK units minus one.

Note: Only CBR refresh is supported

Device 0 Offset 6B - DRAM Arbitration Control.....RW

7-6 Arbitration Parking Policy
- 00 Park at last bus owner.....default
- 01 Park at CPU side
- 10 Park at AGP side
- 11 Reserved

5-1 Reserved ..... always reads 0

0 Multi-Page Open
- 0 Disable (page registers marked invalid and no page register update which causes non page-mode operation)
- 1 Enable (see note † at right) .....default

Device 0 Offset 6C - SDRAM Control ..... RW

7-5 Reserved .....always reads 0

4 DDR Write-to-Read Turnaround
- 0 1T Turnaround (i.e., 3T from Write command to Read command)..... default
- 1 2T Turnaround

3 Single RW Burst Stop Command
- 0 Disable..... default
- 1 Enable BST command to SDRAM to allow fast single-cycle pipeline

2-0 SDRAM Operation Mode Select
- 000 Normal SDRAM Mode..... default
- 001 NOP Command Enable
- 010 All-Banks-Precharge Command Enable (CPU-to-DRAM cycles are converted to All-Banks-Precharge commands).
- 011 MSR Enable
  CPU-to-DRAM cycles are converted to commands and the commands are driven on MA[13:0]. The BIOS selects an appropriate host address for each row of memory such that the right commands are generated on MA[13:0].
- 100 CBR Cycle Enable (if this code is selected, CAS-before-RAS refresh is used; if it is not selected, RAS-Only refresh is used)
- 101 Reserved
- 11x Reserved

Device 0 Offset 6D - DRAM Drive Strength..... RW

7-4 Reserved .....always reads 0

3 SDRAM Command Drive (SRAS#, SCAS#, SWE#)
- 0 16mA ..... default
- 1 24mA

2 MA[2:13] / WE# Drive
- 0 16mA ..... default
- 1 24mA

1 CAS# Drive
- 0 8 mA ..... default
- 1 12 mA

0 RAS# Drive
- 0 16mA ..... default
- 1 24mA

† Note: For SDRAM, Rx68[6], Rx68[7], and Rx6B[0] should all be programmed to 1 and the bank interleave bits in Rx64-66 (bits 1-0) should be set to either 2-way or 4-way interleave. All other combinations are for test purposes only.

Device 0 Offset 6E - ECC Control .....RW

7 ECC / ECMode Select
- 0 ECC Checking and Reporting .....default
- 1 ECC Checking, Reporting, and Correcting

6 Reserved ..... always reads 0

5 Enable SERR# on ECC / EC Multi-Bit Error
- 0 Don't assert SERR# for multi-bit errors..... def
- 1 Assert SERR# for multi-bit errors

4 Enable SERR# on ECC / EC Single-Bit Error
- 0 Don't assert SERR# for single-bit errors..... def
- 1 Assert SERR# for single-bit errors

3 Reserved ..... always reads 0

2 ECC / EC Enable - Bank 5/4 (DIMM 2)
- 0 Disable (no ECC or EC for banks 5/4)...default
- 1 Enable (ECC or EC per bit-7)

1 ECC / EC Enable - Bank 3/2 (DIMM 1)
- 0 Disable (no ECC or EC for banks 3/2)...default
- 1 Enable (ECC or EC per bit-7)

0 ECC / EC Enable - Bank 1/0 (DIMM 0)
- 0 Disable (no ECC or EC for banks 1/0)...default
- 1 Enable (ECC or EC per bit-7)

Error checking / correction may be enabled bank-pair by bank-pair by using bits 0-2 above. Bank pairs must be populated with 72-bit memory to enable for EC or ECC since the additional data bits must be present in either case. For this reason, if 64-bit memory is populated in a particular bank pair, the corresponding bit 0-2 should be set to 0 to disable both EC and ECC for that bank pair. For those bank pairs that have 72-bit memory available (and have the corresponding bit 0-2 set), either EC or ECC may be selected via bit-7 above (i.e., all enabled bank pairs will use EC or all will use ECC).

If error checking / reporting only (EC) is selected, all read and write cycles will use normal timing. Partial writes (with EC or ECC enabled) will use read-modify-write cycles to maintain correct error correction codes in the additional 8 data bits. If EC and ECC are disabled for a particular bank pair, partial writes to that bank pair will use the byte enables to write only the selected bytes (using normal write cycles and cycle timing). If error correction (ECC) is selected, the first read of a transaction will always have one additional cycle of latency.

Bit-7	Bits 2-0	RMW	Error Checking	Error Correction
0/1	0	No	No	No
0	1	Yes	Yes	No
1	1	Yes	Yes	Yes

Device 0 Offset 6F - ECC Status..... RWC

7 Multi-bit (ECC) Error Detected... write of '1' resets

6-4 Multi-bit (ECC) Error DRAM Bank.....default=0
Encoded value of the bank with the multi-bit error.

3 Single-bit (Parity) Error Detected write of '1' resets

2-0 Single-bit (Parity) Error DRAM Bank ....default=0
Encoded value of the bank with the single-bit error.

PCI Bus #1 Control

These registers are normally programmed once at system initialization time.

Device 0 Offset 70 - PCI Buffer Control .....RW

7 CPU to PCI Post-Write
- 0 Disable .....default
- 1 Enable

6 PCI Master to DRAM Post-Write
- 0 Disable .....default
- 1 Enable

5 PCI Master to DRAM Prefetch
- 0 Disable .....default
- 1 Enable

4 Reserved ..... RW

3-1 Reserved ..... always reads 0

0 Delay Transaction Optimization
- 0 Disable .....default
- 1 Enable

Device 0 Offset 71 - CPU to PCI Flow Control 1 ..... RW

7 Dynamic Burst
- 0 Disable..... default
- 1 Enable (see note under bit-3 below)

6 Byte Merge
- 0 Disable..... default
- 1 Enable

5 Reserved .....RW

4 PCI I/O Cycle Post Write
- 0 Disable..... default
- 1 Enable

3 PCI Burst
- 0 Disable..... default
- 1 Enable (bit7=1 will override this option)

bit-7	bit-3	Operation
0	0	Every write goes into the write buffer and no PCI burst operations occur.
0	1	If the write transaction is a burst transaction, the information goes into the write buffer and burst transfers are later performed on the PCI bus. If the transaction is not a burst, PCI write occurs immediately (after a write buffer flush).
1	x	Every write transaction goes to the write buffer; burstable transactions will then burst on the PCI bus and non-burstable won't. This is the normal setting.

2 PCI Fast Back-to-Back Write
- 0 Disable..... default
- 1 Enable

1 Quick Frame Generation
- 0 Disable..... default
- 1 Enable

0 1 Wait State PCI Cycles
- 0 Disable..... default
- 1 Enable

Device 0 Offset 72 - CPU to PCI Flow Control 2.....RW

7 Retry Status over 16 / 64 Times
- 0 No retry occurred .....default
- 1 Retry occurred.....write 1 to clear

6 Retry Timeout Action
- 0 Retry Forever (record status only).....default
- 1 Flush buffer for write or return all 1s for read

5-4 Retry Count and Retry Backoff
- 00 Retry 2 times .....default
- 01 Retry 16 times
- 10 Retry 4 times
- 11 Retry 64 times

3 Clear Failed Data and Continue Retry
- 0 Flush the entire post-write buffer .....default
- 1 When data is posting and master (or target) abort fails, pop the failed data if any, and keep posting

2 CPU Backoff on PCI Read Retry Failure
- 0 Disable .....default
- 1 Backoff CPU when reading data from PCI and retry fails

1 Reduce 1T for FRAME# Generation
- 0 Disable .....default
- 1 Enable

0 Reduce 1T for CPU Read PCI Slave
- 0 Disable .....default
- 1 Enable (bypass TRDY# to LRDY#)

Device 0 Offset 73 - PCI Master Control 1..... RW

7 Reserved .....always reads 0

6 PCI Master 1-Wait-State Write
- 0 Zero wait state TRDY# response..... default
- 1 One wait state TRDY# response

5 PCI Master 1-Wait-State Read
- 0 Zero wait state TRDY# response..... default
- 1 One wait state TRDY# response

4 Reserved .....always reads 0

3 Assert STOP# after PCI Master Write Timeout
- 0 Disable..... default
- 1 Enable

2 Assert STOP# after PCI Master Read Timeout
- 0 Disable..... default
- 1 Enable

1 LOCK# Function
- 0 Disable..... default
- 1 Enable

0 PCI Master Broken Timer Enable
- 0 Disable..... default
- 1 Enable. Force into arbitration when there is no FRAME# 16 PCICLK's after the grant.

Device 0 Offset 74 - PCI Master Control 2..... RW

7 PCI Master Read Prefetch by Enhance Command
- 0 Always Prefetch..... default
- 1 Prefetch only if Enhance command

6 PCI Master Write Merge
- 0 Disable..... default
- 1 Enable

5-0 Reserved .....always reads 0

Device 0 Offset 75 - PCI Arbitration 1 .....RW

7 Arbitration Mechanism
- 0 PCI has priority .....default
- 1 Fair arbitration between PCI and CPU

6 Arbitration Mode
- 0 REQ-based (arbitrate at end of REQ#)...default
- 1 Frame-based (arbitrate at end of each FRAME#)

5-4 Latency Timer ..... read only, reads Rx0D bits 2:1

3-0 PCI Master Bus Time-Out
(force into arbitration after a period of time)
- 0000 Disable .....default
- 0001 1x32 PCICLKs
- 0010 2x32 PCICLKs
- 0011 3x32 PCICLKs
- 0100 4x32 PCICLKs
- ... ...
- 1111 15x32 PCICLKs

Device 0 Offset 76 - PCI Arbitration 2 .....RW

7 Master Priority Rotation Enable
- 0 Disable (arbitration per Rx75 bit-7) .....default
- 1 Enable (arbitration per bits 5-4 of this register) (gives the CPU higher priority than either of the mechanisms defined by Rx75 bit-7). Note: Always set this bit to 1.

6 CPU Latency Timer Bit-0..... RO
- 0 CPU has at least 1 PCLK time slot when CPU has PCI bus
- 1 CPU has no time slot

5-4 Master Priority Rotation Control
- 00 Disabled (arbitration per Rx75 bit-7) .....default
- 01 Grant to CPU after every PCI master grant
- 10 Grant to CPU after every 2 PCI master grants
- 11 Grant to CPU after every 3 PCI master grants

With setting 01, the CPU will always be granted access after the current bus master completes, no matter how many PCI masters are requesting. With setting 10, if other PCI masters are requesting during the current PCI master grant, the highest priority master will get the bus after the current master completes, but the CPU will be guaranteed to get the bus after that master completes. With setting 11, if other PCI masters are requesting, the highest priority will get the bus next, then the next highest priority will get the bus, then the CPU will get the bus. In other words, with the above settings, even if multiple PCI masters are continuously requesting the bus, the CPU is guaranteed to get access after every master grant (01), after every other master grant (10) or after every third master grant (11).

3-0 Reserved ..... always reads 0

Device 0 Offset 77 - Chip Test Mode..... RW

7-6 Reserved (no function) ..... always reads 0
5-0 Reserved (do not use) ..... default=0

Device 0 Offset 7E – DLL Test Mode..... RW

7-6 Reserved (status) .....RO
5-3 Reserved (do not use) ..... default=0
2-0 Reserved (no function) ..... default=0

Device 0 Offset 7F – DLL4 Test Mode..... RW

7-0 Reserved (do not use) ..... default=0

GART / Graphics Aperture Control

The function of the Graphics Address Relocation Table (GART) is to translate virtual 32-bit addresses issued by an AGP device into 4K-page based physical addresses for system memory access. In this translation, the upper 20 bits (A31-A12) are remapped, while the lower 12 address bits (A11-A0) are used unchanged.

A one-level fully associative lookup scheme is used to implement the address translation. In this scheme, the upper 20 bits of the virtual address are used to point to an entry in a page table located in system memory. Each page table entry contains the upper 20 bits of a physical address (a "physical page" address). For simplicity, each page table entry is 4 bytes. The total size of the page table depends on the GART range (called the "aperture size") which is programmable in the VT82C597.

This scheme is shown in the figure below.

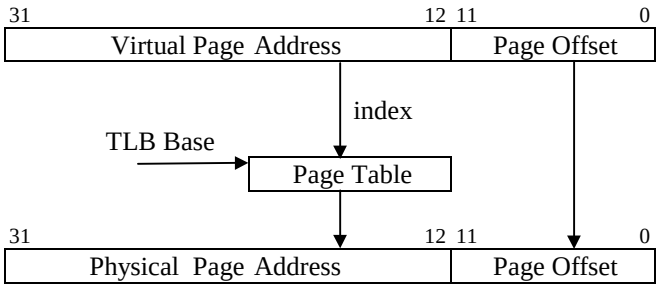


Figure 8. Graphics Aperture Address Translation

Since address translation using the above scheme requires an access to system memory, an on-chip cache (called a "Translation Lookaside Buffer" or TLB) is utilized to enhance performance. The TLB in the 82C597 contains 16 entries. Address "misses" in the TLB require an access of system memory to retrieve translation data. Entries in the TLB are replaced using an LRU (Least Recently Used) algorithm.

Addresses are translated only for accesses within the "Graphics Aperture" (GA). The Graphics Aperture can be any power of two in size from 1MB to 256MB (i.e., 1MB, 2MB, 4MB, 8MB, etc). The base of the Graphics Aperture can be anywhere in the system virtual address space on an address boundary determined by the aperture size (e.g., if the aperture size is 4MB, the base must be on a 4MB address boundary). The Graphics Aperture Base is defined in register offset 10 of device 0. The Graphics Aperture Size and TLB Table Base are defined in the following register group (offsets 84 and 88 respectively) along with various control bits.

Device 0 Offset 83-80 - GART/TLB Control.....RW

31-16 Reserved ..... always reads 0

15-8 Reserved (test mode status)..... RO

7 Flush Page TLB
- 0 Disable .....default
- 1 Enable

6-4 Reserved ..... always reads 0

3 PCI#1 Master Address Translation for GA Access
- 0 Addresses generated by PCI #1 Master accesses of the Graphics Aperture will not be translated .....default
- 1 PCI #1 Master GA addresses will be translated

2 PCI#2 Master Address Translation for GA Access
- 0 Addresses generated by PCI #2 Master accesses of the Graphics Aperture will not be translated .....default
- 1 PCI #2 Master GA addresses will be translated

1 CPU Address Translation for GA Access
- 0 Addresses generated by CPU accesses of the Graphics Aperture will not be translated..... def
- 1 CPU GA addresses will be translated

0 AGP Address Translation for GA Access
- 0 Addresses generated by AGP accesses of the Graphics Aperture will not be translated..... def
- 1 AGP GA addresses will be translated

Note: For any master access to the Graphics Aperture range, snoop will not be performed.

Device 0 Offset 84 - Graphics Aperture Size..... RW

7-0 Graphics Aperture Size
- 11111111 1M
- 11111110 2M
- 11111100 4M
- 11111000 8M
- 11110000 16M
- 11100000 32M
- 11000000 64M
- 10000000 128M
- 00000000 256M

3-0 Reserved .....always reads 0

Offset 8B-88 - GA Translation Table Base..... RW

31-12 Graphics Aperture Translation Table Base. Pointer to the base of the translation table in system memory used to map addresses in the aperture range (the pointer to the base of the "Directory" table).

11-2 Reserved .....always reads 0

1 Graphics Aperture Enable
- 0 Disable..... default
- 1 Enable

Note: To disable the Graphics Aperture, set this bit to 0 and set all bits of the Graphics Aperture Size to 0. To enable the Graphics Aperture, set this bit to 1 and program the Graphics Aperture Size to the desired aperture size.

0 Translation Table Noncachable
- 0 Cachable ..... default
- 1 Non-cachable

Note: Setting this bit will make the address range programmed in bits 31-12 of this register non-cachable to L1/L2 with the following bits masked per the Graphics Aperture Size (offset 84 described above):
- Address bit 17 masked if Size bit-7 = 0
- Address bit 16 masked if Size bit-6 = 0
- Address bit 15 masked if Size bit-5 = 0
- Address bit 14 masked if Size bit-4 = 0
- Address bit 13 masked if Size bit-3 = 0
- Address bit 12 masked if Size bit-2 = 0
- Address bit 11 masked if Size bit-1 = 0
- Address bit 10 masked if Size bit-0 = 0

Note: If TLB miss, the TLB table is fetched by the address:

Gr Ap Trans Table Base [31:12] + A[27:22], A[21:12], 2'b00

AGP Control

Device 0 Offset A3-A0 - AGP Capability Identifier .....RO

31-24 Reserved ..... always reads 00
23-20 Major Specification Revision ..... always reads 0001
Major revision # of AGP spec device conforms to
19-16 Minor Specification Revision ..... always reads 0000
Minor revision # of AGP spec device conforms to
15-8 Pointer to Next Item..... always reads 00 (last item)
7-0 AGP ID .. (always reads 02 to indicate it is AGP)

Device 0 Offset A7-A4 - AGP Status.....RO

31-24 Maximum AGP Requests ..... always reads 07
Max # of AGP requests the device can manage (8)
23-10 Reserved .....always reads 0s
9 Supports SideBand Addressing ..... always reads 1
8-2 Reserved .....always reads 0s
1 2X Rate Supported..... always reads 1
0 1X Rate Supported..... always reads 1

Device 0 Offset AB-A8 - AGP Command.....RW

31-24 Request Depth (reserved for target)...always reads 0s
23-10 Reserved .....always reads 0s
9 SideBand Addressing Enable
0 Disable .....default
1 Enable
8 AGP Enable
0 Disable .....default
1 Enable
7-2 Reserved .....always reads 0s
1 2X Mode Enable
0 Disable .....default
1 Enable
0 1X Mode Enable
0 Disable .....default
1 Enable

Device 0 Offset AC - AGP Control..... RW

7-3 Reserved ..... always reads 0s
2 LPR In-Order Access (Force Fence)
0 Fence/Flush functions not guaranteed. AGP read requests (low/normal priority and high priority) may be executed before previously issued write requests. ..... default
1 Force all requests to be executed in order (automatically enables Fence/Flush functions). Low (i.e., normal) priority AGP read requests will never be executed before previously issued writes. High priority AGP read requests may still be executed prior to previously issued write requests as required.
1 Reserved (always write 0)..... R/W, default=0
0 Fast Response for Low Priority Read
0 Wait for data of entire transaction is received before grant is generated..... default
1 Generate grant immediately after first block of data is received

Device 1 Header Registers - PCI-to-PCI Bridge

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number of 0 and function number equal to 0 and device number equal to one.

Device 1 Offset 1-0 - Vendor ID ..... RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 1 Offset 3-2 - Device ID ..... RO

15-0 ID Code (reads 8597h to identify the VT82C597 PCI-to-PCI Bridge device)

Device 1 Offset 5-4 - Command ..... RW

15-10 Reserved ..... always reads 0

9 Fast Back-to-Back Cycle Enable ..... RO
- 0 Fast back-to-back transactions only allowed to the same agent ..... default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable ..... RO
- 0 SERR# driver disabled ..... default
- 1 SERR# driver enabled

(SERR# is used to report parity errors if bit-6 is set).

7 Address / Data Stepping ..... RO
- 0 Device never does stepping ..... default
- 1 Device always does stepping

6 Parity Error Response ..... RW
- 0 Ignore parity errors & continue ..... default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop ..... RO
- 0 Treat palette accesses normally ..... default
- 1 Don't respond to palette writes on PCI bus (10-bit decode of I/O addresses 3C6-3C9 hex)

4 Memory Write and Invalidate Command ..... RO
- 0 Bus masters must use Mem Write ..... default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring ..... RO
- 0 Does not monitor special cycles ..... default
- 1 Monitors special cycles

2 Bus Master ..... RW
- 0 Never behaves as a bus master
- 1 Enable to operate as a bus master on the primary interface on behalf of a master on the secondary interface ..... default

1 Memory Space ..... RW
- 0 Does not respond to memory space
- 1 Enable memory space access ..... default

0 I/O Space ..... RW
- 0 Does not respond to I/O space
- 1 Enable I/O space access ..... default

Device 1 Offset 7-6 - Status (Primary Bus) ..... RWC

15 Detected Parity Error ..... always reads 0

14 Signaled System Error (SERR#) ..... always reads 0

13 Signaled Master Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the master with Master-Abort (except Special Cycles) ..... write 1 to clear

12 Received Target Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the target with Target-Abort ..... write 1 to clear

11 Signaled Target Abort ..... always reads 0

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium ..... always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected ..... always reads 0

7 Fast Back-to-Back Capable ..... always reads 0

6 User Definable Features ..... always reads 0

5 66MHz Capable ..... always reads 1

4 Supports New Capability list ..... always reads 0

3-0 Reserved ..... always reads 0

Device 1 Offset 8 - Revision ID ..... RO

7-0 VT82C597 Chip Revision Code (00=First Silicon)

Device 1 Offset 9 - Programming Interface ..... RO

This register is defined in different ways for each Base/Sub-Class Code value and is undefined for this type of device.

7-0 Interface Identifier ..... always reads 00

Device 1 Offset A - Sub Class Code ..... RO

7-0 Sub Class Code .reads 04 to indicate PCI-PCI Bridge

Device 1 Offset B - Base Class Code ..... RO

7-0 Base Class Code .. reads 06 to indicate Bridge Device

Device 1 Offset D - Latency Timer ..... RO

7-0 Reserved ..... always reads 0

Device 1 Offset E - Header Type ..... RO

7-0 Header Type Code ..... reads 01: PCI-PCI Bridge

Device 1 Offset F - Built In Self Test (BIST) ..... RO

7 BIST Supported ..... reads 0: no supported functions

6 Start Test ..... write 1 to start but writes ignored

5-4 Reserved ..... always reads 0

3-0 Response Code ..... 0 = test completed successfully

Device 1 Offset 18 - Primary Bus Number .....RW

7-0 Primary Bus Number..... default = 0

This register is read write, but internally the chip always uses bus 0 as the primary.

Device 1 Offset 19 - Secondary Bus Number .....RW

7-0 Secondary Bus Number..... default = 0

Note: PCI#2 must use these bits to convert Type 1 to Type 0.

Device 1 Offset 1A - Subordinate Bus Number .....RW

7-0 Primary Bus Number..... default = 0

Note: PCI#2 must use these bits to decide if Type 1 to Type 1 command passing is allowed.

Device 1 Offset 1C - I/O Base .....RW

7-4 I/O Base AD[15:12]..... default = 1111b

3-0 I/O Addressing Capability..... default = 0

Device 1 Offset 1D - I/O Limit.....RW

7-4 I/O Limit AD[15:12] ..... default = 0

3-0 I/O Addressing Capability..... default = 0

Device 1 Offset 1F-1E - Secondary Status ..... RO

15-0 Reserved .....always reads 0000

Device 1 Offset 21-20 - Memory Base ..... RW

15-4 Memory Base AD[31:20] ..... default = 0FFFh

3-0 Reserved .....always reads 0

Device 1 Offset 23-22 - Memory Limit (Inclusive)..... RW

15-4 Memory Limit AD[31:20] .....default = 0

3-0 Reserved .....always reads 0

Device 1 Offset 25-24 - Prefetchable Memory Base..... RW

15-4 Prefetchable Memory Base AD[31:20] def = 0FFFh

3-0 Reserved .....always reads 0

Device 1 Offset 27-26 - Prefetchable Memory Limit ..... RW

15-4 Prefetchable Memory Limit AD[31:20].....
.....default = 0

3-0 Reserved .....always reads 0

Device 1 Offset 3F-3E – PCI-to-PCI Bridge Control..... RW

15-4 Reserved .....always reads 0

3 VGA-Present on AGP

0 Forward VGA accesses to PCI Bus #1 .. default

1 Forward VGA accesses to PCI Bus #2 / AGP

Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use Axxxxh. Mono VGA uses I/O addresses 3Bx-3Cxh and Color VGA uses 3Cx-3Dxh. If an MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.

2 Block / Forward ISA I/O Addresses

0 Forward all I/O accesses to the AGP bus if they are in the range defined by the I/O Base and I/O Limit registers (device 1 offset 1C-1D) .....default

1 Do not forward I/O accesses to the AGP bus that are in the 100-3FFh address range even if they are in the range defined by the I/O Base and I/O Limit registers.

1-0 Reserved .....always reads 0

Device 1 Configuration Registers - PCI-to-PCI Bridge

PCI Bus #2 Control

Device 1 Offset 40 - CPU-to-PCI #2 Flow Control 1..RW

7 CPU-PCI #2 Post Write
- 0 Disable .....default
- 1 Enable

6 CPU-PCI #2 Dynamic Burst
- 0 Disable .....default
- 1 Enable

5 CPU-PCI #2 One Wait State Burst Write
- 0 Disable .....default
- 1 Enable

4-3 Reserved ..... default = 0

2 MDA Present on PCI #2
- 0 Forward MDA accesses to AGP.....default
- 1 Forward MDA accesses to PCI #1

Note: Forward despite IO / Memory Base / Limit

Note: MDA (Monochrome Display Adapter) addresses are memory addresses B0000h-B7FFFh and I/O addresses 3B4-3B5h, 3B8-3BAh, and 3BFh (10-bit decode). 3BC-3BE are reserved for printers.

Note: If Rx3E bit-3 is 0, this bit is a don't care (MDA accesses are forwarded to the PCI bus).

1-0 Reserved ..... default = 0

Table 6. VGA/MDA Memory/IO Redirection

3E[3] VGA Pres.	40[2] MDA Pres.	VGA is on	MDA is on	Axxxx, B8xxx Access	B0000 -B7FFF Access	3Cx, 3Dx I/O	3Bx I/O
0	-	PCI	PCI	PCI	PCI	PCI	PCI
1	0	AGP	AGP	AGP	AGP	AGP	AGP
1	1	AGP	PCI	AGP	PCI	AGP	PCI

Device 1 Offset 41 - CPU-to-PCI #2 Flow Control 2 ..... RW

7 Retry Status
- 0 No retry occurred..... default
- 1 Retry Occurred (write 1 to clear)

7 Retry Timeout Action
- 0 No action taken except to record status ..... def
- 1 Flush buffer for write or return all 1s for read

5-4 Retry Count
- 00 Retry 2, backoff CPU ..... default
- 01 Retry 4, backoff CPU
- 10 Retry 16, backoff CPU
- 11 Retry 64, backoff CPU

3 Post Write Data on Abort
- 0 Flush entire post-write buffer on target-abort or master abort..... default
- 1 Pop one data output on target-abort or master-abort

2 CPU Backoff on PCI #2 Read Retry Timeout
- 0 Disable..... default
- 1 Enable

1-0 Reserved .....always reads 0

Device 1 Offset 42 - PCI #2 Master Control..... RW

7 Read Prefetch for Enhance Command
- 0 Always Perform Prefetch..... default
- 1 Prefetch only if Enhance Command

6 PCI #2 Master One Wait State Write
- 0 Disable..... default
- 1 Enable

5 PCI #2 Master One Wait State Read
- 0 Disable..... default
- 1 Enable

4 Reserved .....always reads 0

3 PCI #2 Master Write Timeout Asserts STOP#
- 0 Disable..... default
- 1 Enable

2 PCI #2 Master Read Timeout Asserts STOP#
- 0 Disable..... default
- 1 Enable

1-0 Reserved .....always reads 0

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Ambient operating temperature	0	70	^{O}C
Storage temperature	-55	125	^{O}C
Input voltage	-0.5	5.5	Volts
Output voltage (V_{DD} = 3.1 - 3.6V)	-0.5	V_{DD} + 0.5	Volts

Note: Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

DC Characteristics

TA-0-70^{O}C, V_{DD}=5V+/-5%, GND=0V

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input low voltage	-0.50	0.8	V	
V_{IH}	Input high voltage	2.0	V_{DD}+0.5	V	
V_{OL}	Output low voltage	-	0.45	V	I_{OL}=4.0mA
V_{OH}	Output high voltage	2.4	-	V	I_{OH}=-1.0mA
I_{IL}	Input leakage current	-	+/-10	uA	$0<V_{IN}<V_{DD}$
I_{OZ}	Tristate leakage current	-	+/-20	uA	$0.45<V_{OUT}<V_{DD}$
I_{CC}	Power supply current	-		mA	

AC Timing Specifications

AC timing specifications provided are based on external zero-pf capacitance load. Min/max cases are based on the following table:

Table 7. AC Timing Min / Max Conditions

Parameter	Min	Max	Unit
3.3V Power (VDD3)	3.135	3.465	Volts
5V Power (VDD5)	4.75	5.25	Volts
Temperature	0	70	^{O}C

Table 8. AC Characteristics - CPU Cycle Timing

Parameter	Min	Max	Unit	Notes
ADS# Setup Time to CCLK Rising	4.2		ns	0pf
W/R# Setup Time to CCLK Rising	4.0		ns	
M/IO# Setup Time to CCLK Rising	4.5		ns	
D/C# Setup Time to CCLK Rising	1.5		ns	
BE[7:0]# Setup Time to CCLK Rising	1.2		ns	
HITM# Setup Time to CCLK Rising	4.2		ns	
CACHE# Setup Time to CCLK Rising	1.1		ns	
HA[31:3] Setup Time to CCLK Rising	3.3		ns	
LOCK# Setup Time to CCLK Rising	3.8		ns	
ADS# Hold Time to CCLK Rising	0.8		ns	
W/R# Hold Time to CCLK Rising	0.7		ns	
M/IO# Hold Time to CCLK Rising	0.7		ns	
D/C# Hold Time to CCLK Rising	0.8		ns	
BE[7:0]# Hold Time to CCLK Rising	0.9		ns	
HITM# Hold Time to CCLK Rising	0.8		ns	
CACHE# Hold time to CCLK Rising	0.8		ns	
HA[31:3] Hold Time to CCLK Rising	0.9		ns	
BRDY# Valid Delay From CCLK Rising	1.9	4.9	ns	
NA# Valid Delay From CCLK Rising	1.6	4.2	ns	
AHOLD Valid Delay From CCLK Rising	1.8	4.6	ns	
BOFF# Valid Delay From CCLK Rising	1.8	4.8	ns	
EADS# Valid Delay From CCLK Rising	1.8	4.6	ns	
KEN#/INV# Valid Delay from CCLK Rising	1.8	4.8	ns	
BE[7:0]# Valid Delay from CCLK Rising	1.6	4.1	ns	
HA[31:3] Valid Delay from CCLK Rising	2.4	6.2	ns	

Table 9. AC Characteristics - L2 Cache Timing

Parameter	Min	Max	Unit	Notes
COE# Valid Delay from CCLK Rising	1.7	4.5	ns	0pf
TA[9:0] Valid Delay from CCLK Rising	2.6	6.1	ns	
TWE# Valid Delay from CCLK Rising	1.6	4.3	ns	
GWE# Valid Delay from CCLK Rising	1.5	4.0	ns	
BWE# Valid Delay from CCLK Rising	1.5	3.9	ns	
CADS# Valid Delay from CCLK Rising	1.7	4.4	ns	
CADV# Valid Delay from CCLK Rising	1.7	4.2	ns	
TA[9:0] setup time to CCLK Rising	6.0		ns	
TA[9:0] Hold Time from CCLK Rising	0.5		ns	

Table 10. AC Characteristics – DRAM Interface Timing

Parameter	Min	Max	Unit	Notes
RAS[5:0]# Valid Delay from CCLK Rising (EDO)	2.6	5.8	ns	0pf
CS[5:0]# Valid Delay from CCLK Rising (SDRAM)	2.5	6.3	ns	
CAS[7:0]# Valid Delay from CCLK Rising (EDO)	2.0	5.2	ns	
DQM[7:0]# Valid Delay from CCLK Rising (SDRAM)	2.0	5.2	ns	
SRAS[A,B,C]# Valid Delay from CCLK Rising (SDRAM)	1.5	3.8	ns	
SCAS[A,B,C]# Valid Delay from CCLK Rising (SDRAM)	1.4	3.7	ns	
SWE[A,B,C]# Valid Delay from CCLK Rising (SDRAM)	1.6	4.1	ns	
MA[11:2] Valid Delay from CCLK Rising on first Clock after RAS# asserts	2.3	5.9	ns	
MA[1:0] Valid Delay from CCLK Rising (burst)	2.4	6.2	ns	
MA[11:0] Flow Through Delay from HA for first read cycle	5.0	12.8	ns	
SWE[A,B,C]# Valid Delay from CCLK Rising (EDO)	2.8	7.3	ns	

Table 11. AC Characteristics - Data Timing

Parameter	Min	Max	Unit	Notes
HD Valid Delay from CCLK Rising	1.7	4.4	ns	0pf
HD Setup Time to CCLK Rising	2.9		ns	
HD Hold Time from CCLK Rising	0.7		ns	
MD Valid Delay from CCLK Rising	2.2	5.6	ns	
MD Setup Time to CCLK Rising (SDRAM)	0.6		ns	
MD Setup Time to CCLK Falling (EDO)	2.2		ns	
MD Hold Time from CCLK Rising (SDRAM)	1.2		ns	
MD Hold Time from CCLK Falling (EDO)	3.1		ns	

Table 12. AC Characteristics - PCI Cycle Timing

Parameter	Min	Max	Unit	Notes
AD[31:0] Valid Delay from PCLK Rising (address phase)	5.0	11	ns	50pf
AD[31:0] Valid Delay from PCLK Rising (data phase)	5.0	11	ns	
AD[31:0] Setup Time to CCLK Rising	1.5		ns	
AD[31:0] Hold Time to CCLK Rising	0.8		ns	
CBE[3:0]# Setup Time to CCLK Rising	1.0		ns	
FRAME# Setup Time to CCLK Rising	5.8		ns	
TRDY# Setup Time to CCLK Rising	5.5		ns	
IRDY# Setup Time to CCLK Rising	5.0		ns	
STOP# Setup Time to CCLK Rising	3.8		ns	
DEVSEL# Setup Time to CCLK Rising	4.8		ns	
REQ[3:0]# Setup Time to CCLK Rising	8.7		ns	
CBE[3:0]# Hold Time to CCLK Rising	0.2		ns	
FRAME# Hold Time to CCLK Rising	0.3		ns	
TRDY# Hold Time to CCLK Rising	0.4		ns	
IRDY# Hold Time to CCLK Rising	0.3		ns	
STOP# Hold Time to CCLK Rising	0.8		ns	
DEVSEL# Hold Time to CCLK Rising	0.3		ns	
REQ[3:0]# Hold Time to CCLK Rising	0.8		ns	
CBE[3:0]# Valid Delay from PCLK Rising	2.9	7.5	ns	
FRAME# Valid Delay from PCLK Rising	2.8	7.3	ns	
TRDY# Valid Delay from PCLK Rising	5.8	15.0	ns	
IRDY# Valid Delay from PCLK Rising	2.9	7.5	ns	
STOP# Valid Delay from PCLK Rising	2.9	7.5	ns	
DEVSEL# Valid Delay from PCLK Rising	2.8	7.3	ns	
GNT[3:0]#, Valid Delay from PCLK Rising	2.3	6.0	ns	
CBE[3:0]# ,Float Delay from CCLK Rising	3.4	8.7	ns	
FRAME# ,Float Delay from CCLK Rising	3.4	9.8	ns	
TRDY# ,Float Delay from CCLK Rising	3.8	10.0	ns	
IRDY# ,Float Delay from CCLK Rising	3.9	10.0	ns	
STOP# ,Float Delay from CCLK Rising	3.4	9.8	ns	
DEVSEL# ,Float Delay from CCLK Rising	3.8	9.9	ns	

Table 13. AC Characteristics – PCI-66 Cycle Timing

Parameter	Min	Max	Unit	Notes
AD[31:0] Valid Delay from CCLK Rising (address phase)	3.1	5.4	ns	0pf
AD[31:0] Valid Delay from CCLK Rising (data phase)	3.1	5.4	ns	
AD[31:0] Setup Time to CCLK Rising	1.4		ns	
AD[31:0] Hold Time to CCLK Rising	0.3		ns	
CBE[3:0]# Setup Time to CCLK Rising	0.9		ns	
FRAME# Setup Time to CCLK Rising	4.0		ns	
TRDY# Setup Time to CCLK Rising	2.0		ns	
IRDY# Setup Time to CCLK Rising	4.5		ns	
STOP# Setup Time to CCLK Rising	2.7		ns	
DEVSEL# Setup Time to CCLK Rising	4.4		ns	
CBE[3:0]# Hold Time to CCLK Rising	0.4		ns	
FRAME# Hold Time to CCLK Rising	0.6		ns	
TRDY# Hold Time to CCLK Rising	0.4		ns	
IRDY# Hold Time to CCLK Rising	0.2		ns	
STOP# Hold Time to CCLK Rising	0.7		ns	
DEVSEL# Hold Time to CCLK Rising	0.4		ns	
CBE[3:0]# Valid Delay from CCLK Rising	2.1	5.3	ns	
FRAME# Valid Delay from CCLK Rising	2.1	5.2	ns	
TRDY# Valid Delay from CCLK Rising	2.1	5.3	ns	
IRDY# Valid Delay from CCLK Rising	2.1	5.4	ns	
STOP# Valid Delay from CCLK Rising	2.1	5.2	ns	
DEVSEL# Valid Delay from CCLK Rising	2.1	5.6	ns	
GNT#, Valid Delay from CCLK Rising	2.5	5.2	ns	
CBE[3:0]# ,Float Delay from CCLK Rising	3.3	11	ns	
FRAME# ,Float Delay from CCLK Rising	1.7	7	ns	
TRDY# ,Float Delay from CCLK Rising	1.7	7	ns	
IRDY# ,Float Delay from CCLK Rising	3.3	11	ns	
STOP# ,Float Delay from CCLK Rising	1.7	7	ns	
DEVSEL# ,Float Delay from CCLK Rising	2.1	8	ns	

Table 14. AC Characteristics - AGP (1X) Cycle Timing

Parameter	Min	Max	Unit	Notes
GD[31:0] Valid delay from CCLK Rising (request phase)	1.1	5.2	ns	0 pf
GD[31:0] Valid delay from CCLK Rising (data phase)	0.2		ns	
GD[31:0] Valid delay from CCLK Rising (data phase)	2.0	5.0	ns	
GD[31:0] Hold Time to CCLK Rising	0.6		ns	
GBE[3:0]#, Setup Time to CCLK Rising	5.0		ns	
GPIPE#, Setup Time to CCLK Rising	3.6		ns	
SBA[7:0], Setup Time to CCLK Rising	4.7		ns	
GIRDY#, Setup Time to CCLK Rising	4.7		ns	
GRBF#, Setup Time to CCLK Rising	4.7		ns	
CBE[3:0]#, Hold Time from CCLK Rising	0.8		ns	
GPIPE#, Hold Time from CCLK Rising	0.3		ns	
SBA[7:0], Hold Time from CCLK Rising	0.2		ns	
GIRDY#, Hold Time from CCLK Rising	0.3		ns	
GRBF#, Hold Time from CCLK Rising	0.1		ns	
ST[2:0], valid Delay from CCLK Rising	2.4	5.5	ns	
GTRDY#, Valid Delay from CCLK Rising	2.6	5.7	ns	
RREQ# Setup Time to CCLK Rising	3.5		ns	
GREQ# Hold Time to CCLK Rising	0.3		ns	
GGNT# Valid Delay from CCLK Rising	1.5	5.5	ns	

Table 15. AC Characteristics - AGP (2X) Cycle Timing

Parameter	Min	Max	Unit	Notes
GD[31:0] Setup Time to GDS[1:0]#	0.4		ns	0 pf
GBE[3:0]# Setup Time to GDS[1:0]#	0.4		ns	
SBA[7:0] Setup Time to SBS#	0.7		ns	
GDS[1:0]# to CCLK Rising (T2) Setup Time	0.7		ns	
SBS# to CCLK Rising Setup Time	0.7		ns	
GD[31:0] Hold Time from to GDS[1:0]# falling	0.7		ns	
GBE[3:0]# Hold Time from to GDS[1:0]# falling	0.7		ns	
SBA[7:0] Hold Time from to SBS# falling	0.4		ns	
GDS[1:0]# to CCLK Rising (T2) Hold Time	1.5		ns	
SBS# to CCLK Rising Hold Time	1.5		ns	
GD[31:0] Valid Delay before GDS[1:0]#	1.8	3.7	ns	
GD[31:0] Valid Delay after GDS[1:0]#	1.8	3.8	ns	
GD[31:0] Float to Active Delay	2.0	5.2	ns	
GD[31:0] Active to Float Delay	1.7	4.4	ns	
GDS[1:0]# Falling Delay from CCLK Rising	3.4	8.9	ns	
GDS[1:0]# Rising Delay from CCLK Rising	6.0	15.6	ns	

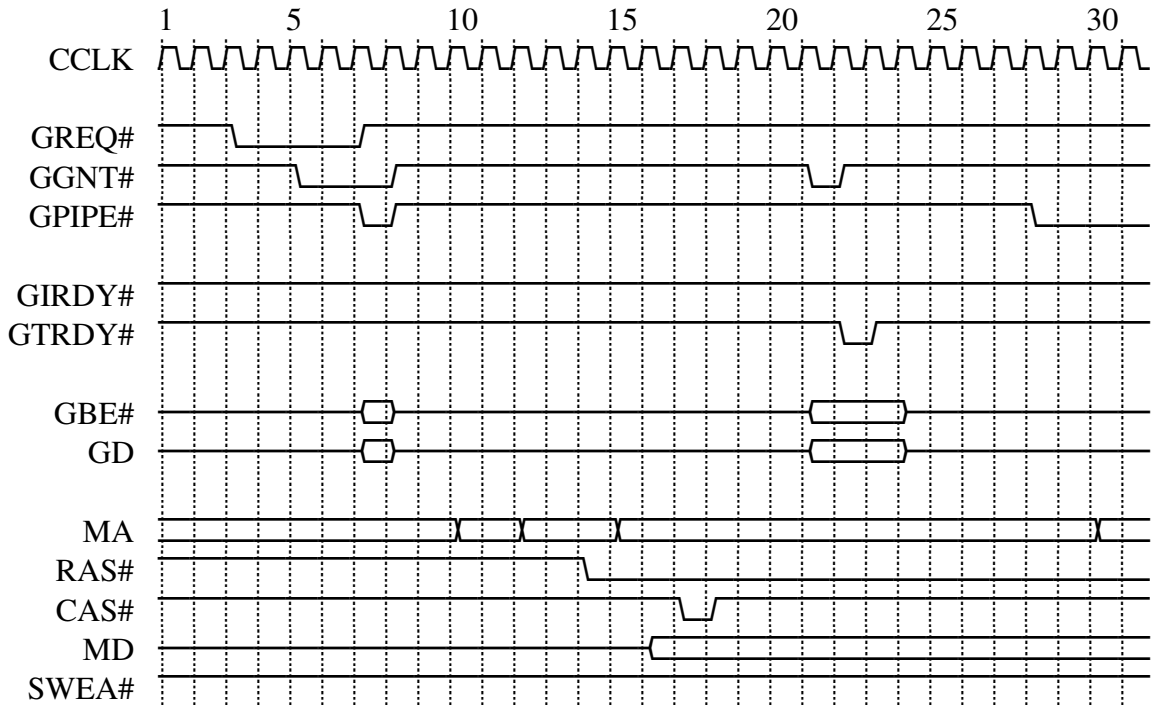


Figure 9. AGP Memory Access (LPR)

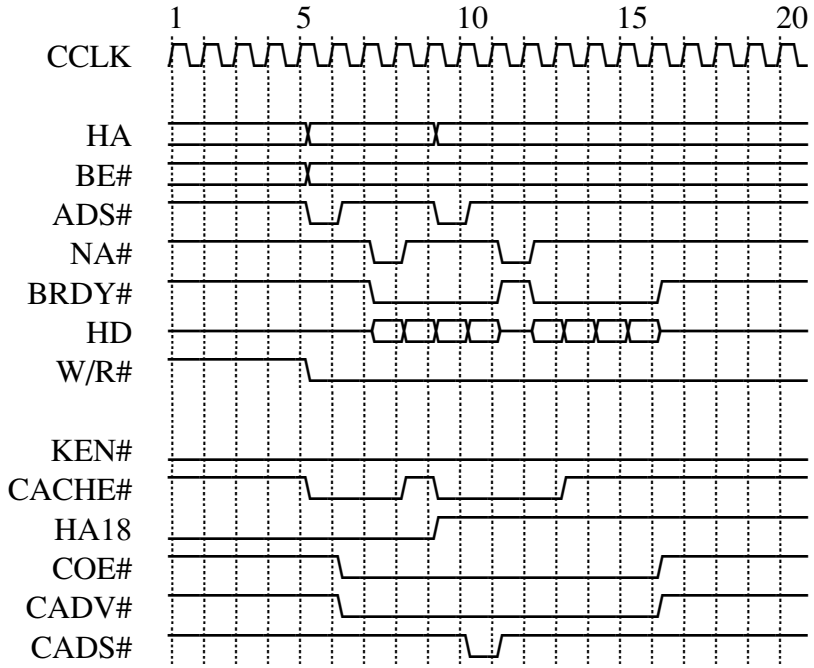


Figure 10. 2-Bank PBSRAM Read 3111-2111

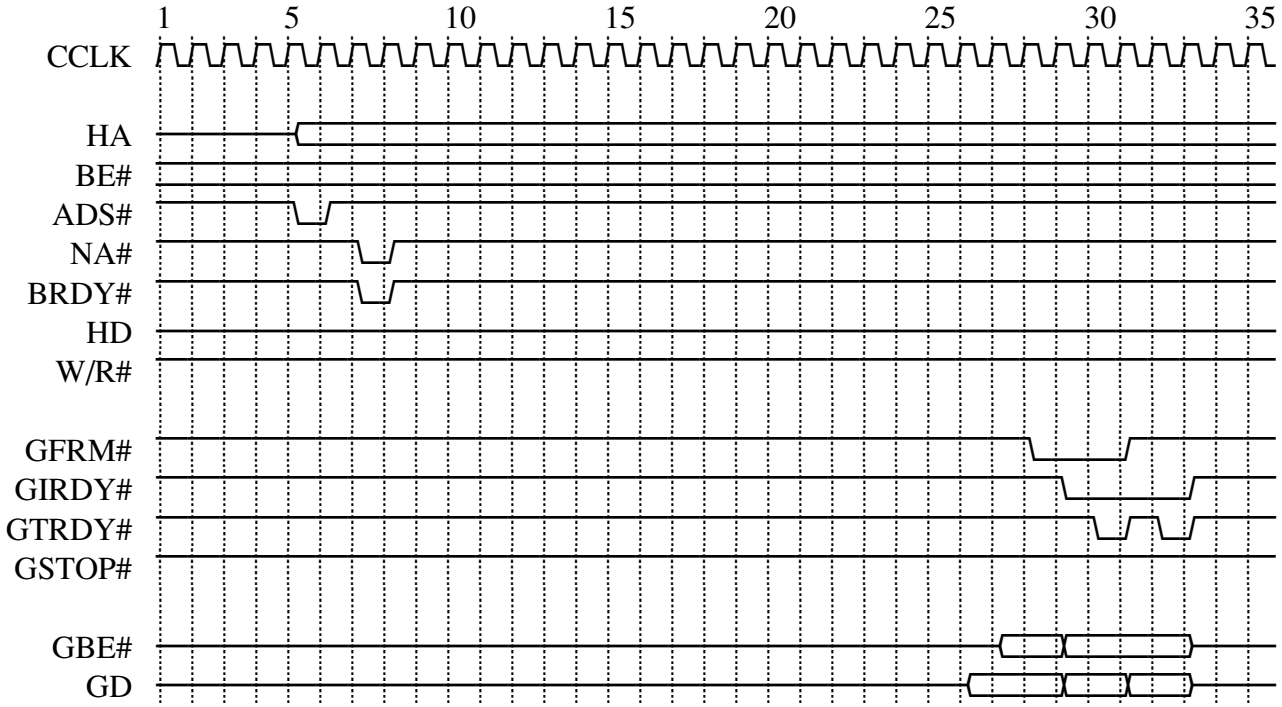


Figure 11. PCI-66 Configuration Cycle

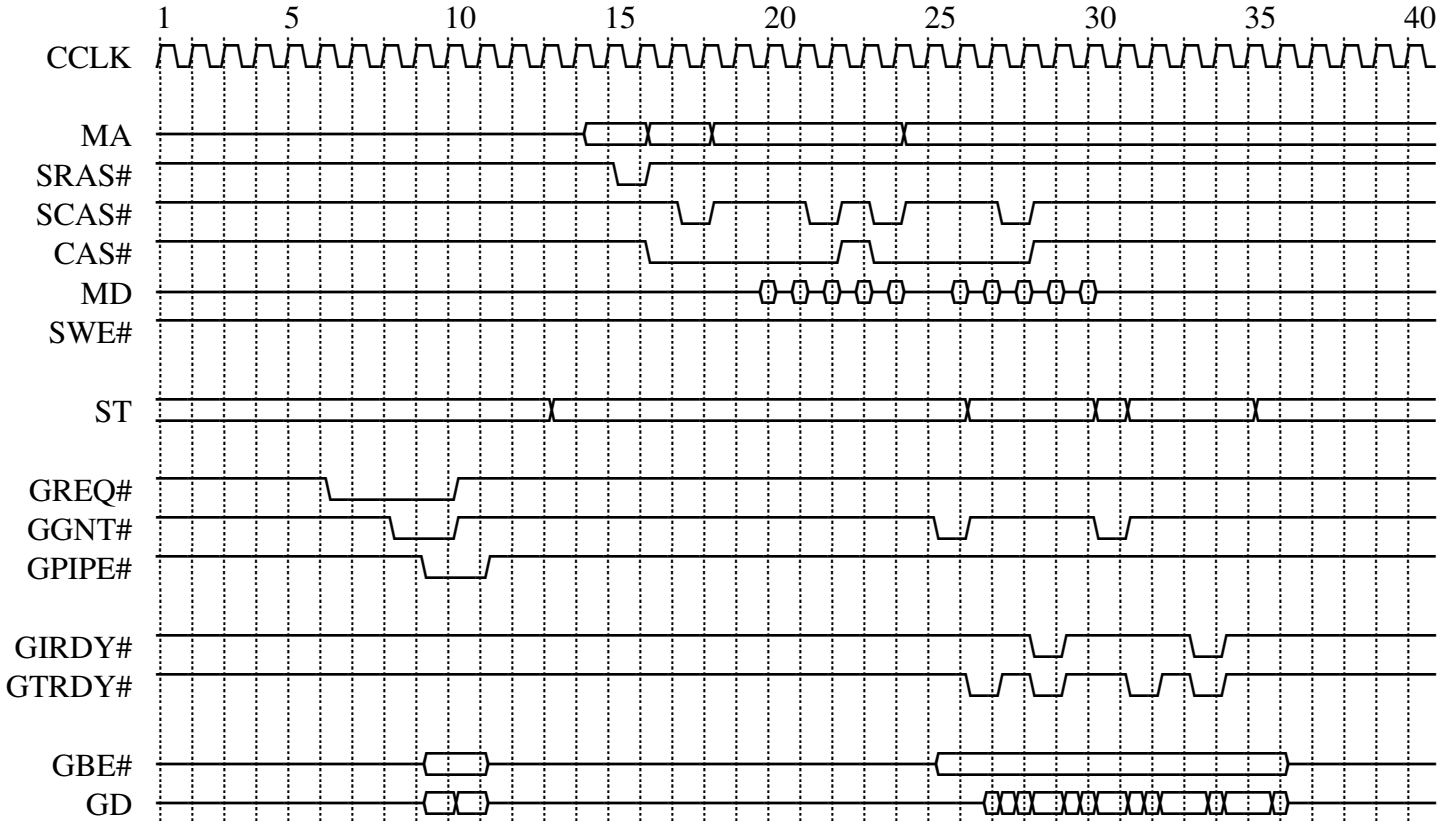


Figure 12. AGP Read SDRAM (2L) 1x Pipe Mode

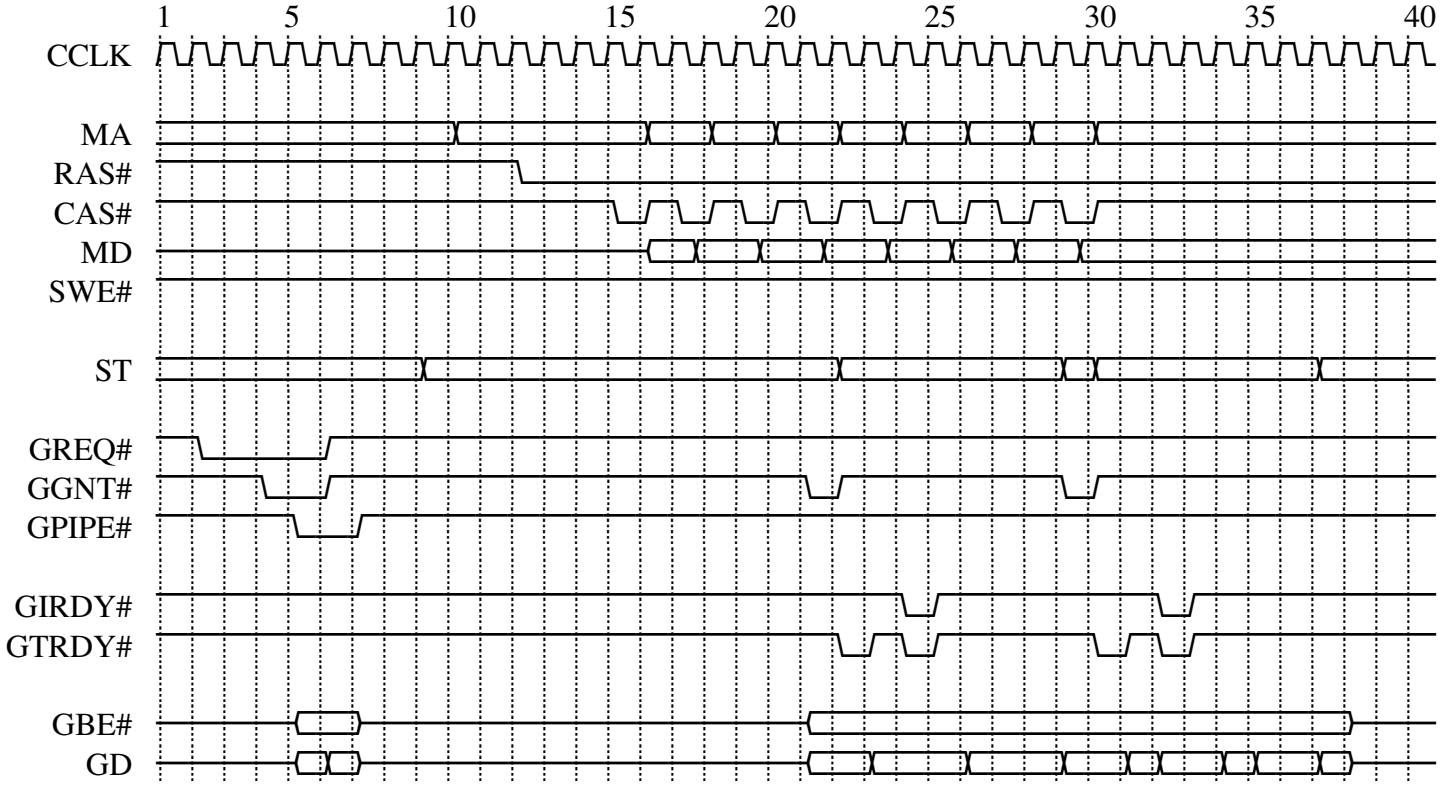


Figure 13. AGP Read EDO 1x Pipe Mode

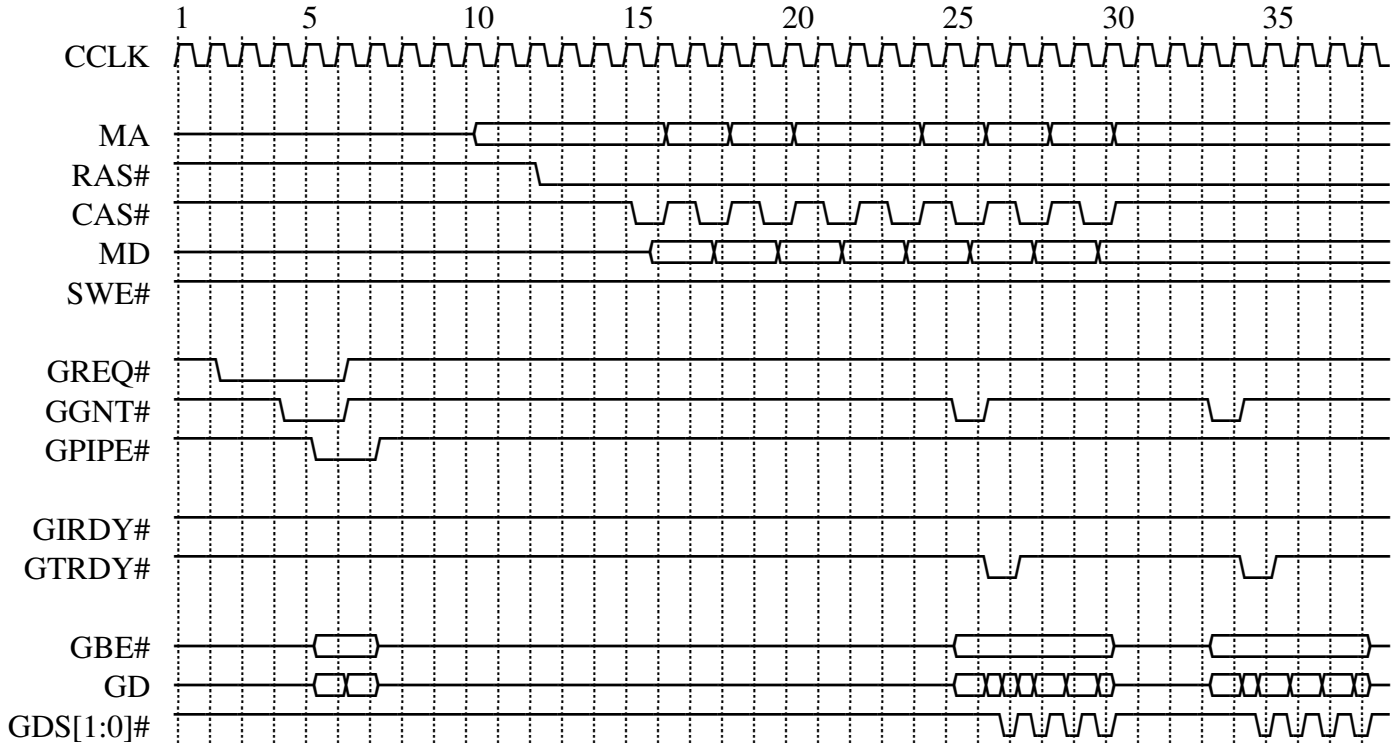


Figure 14. AGP Read EDO PIPE 2x Mode

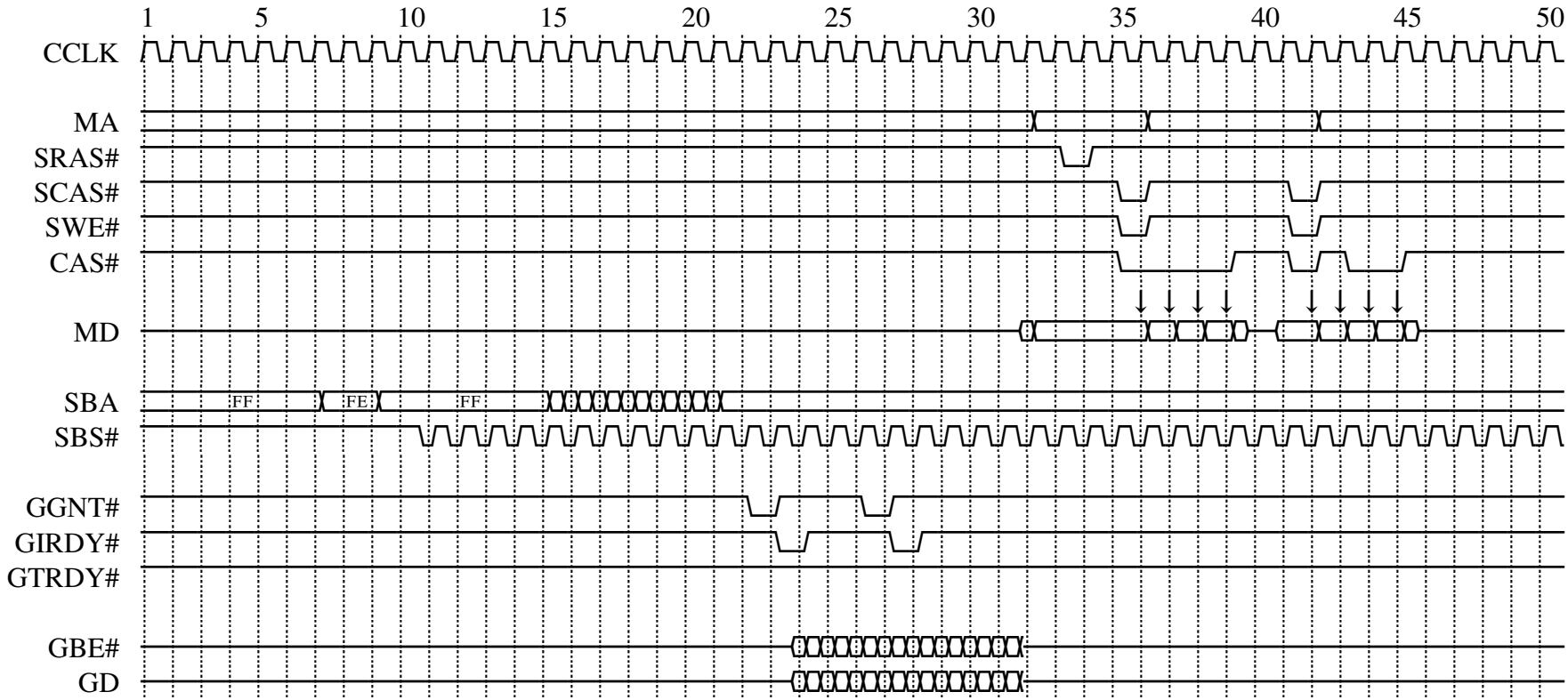


Figure 15. AGP Sideband Address 2x Write SDRAM

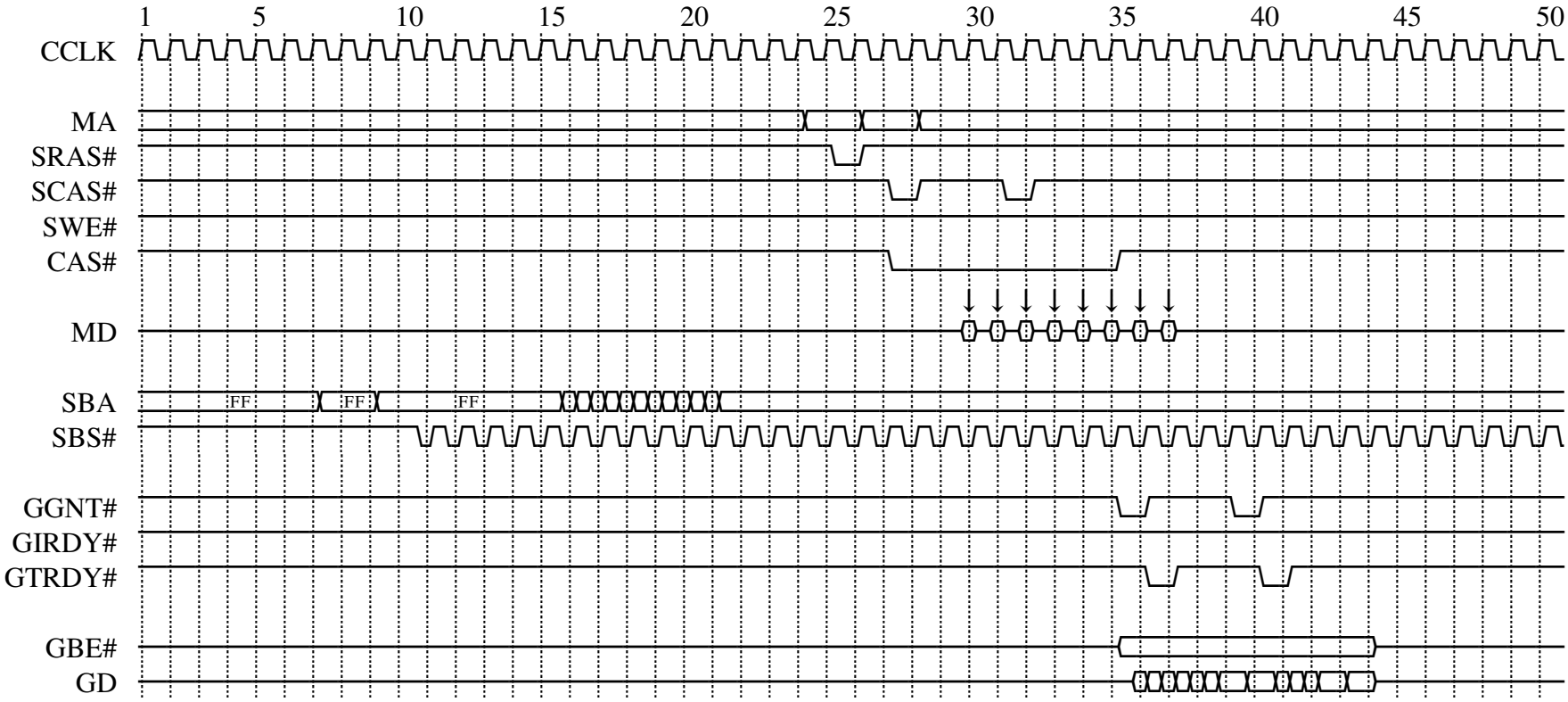


Figure 16. AGP Sideband Address 2x Read SDRAM (2L)

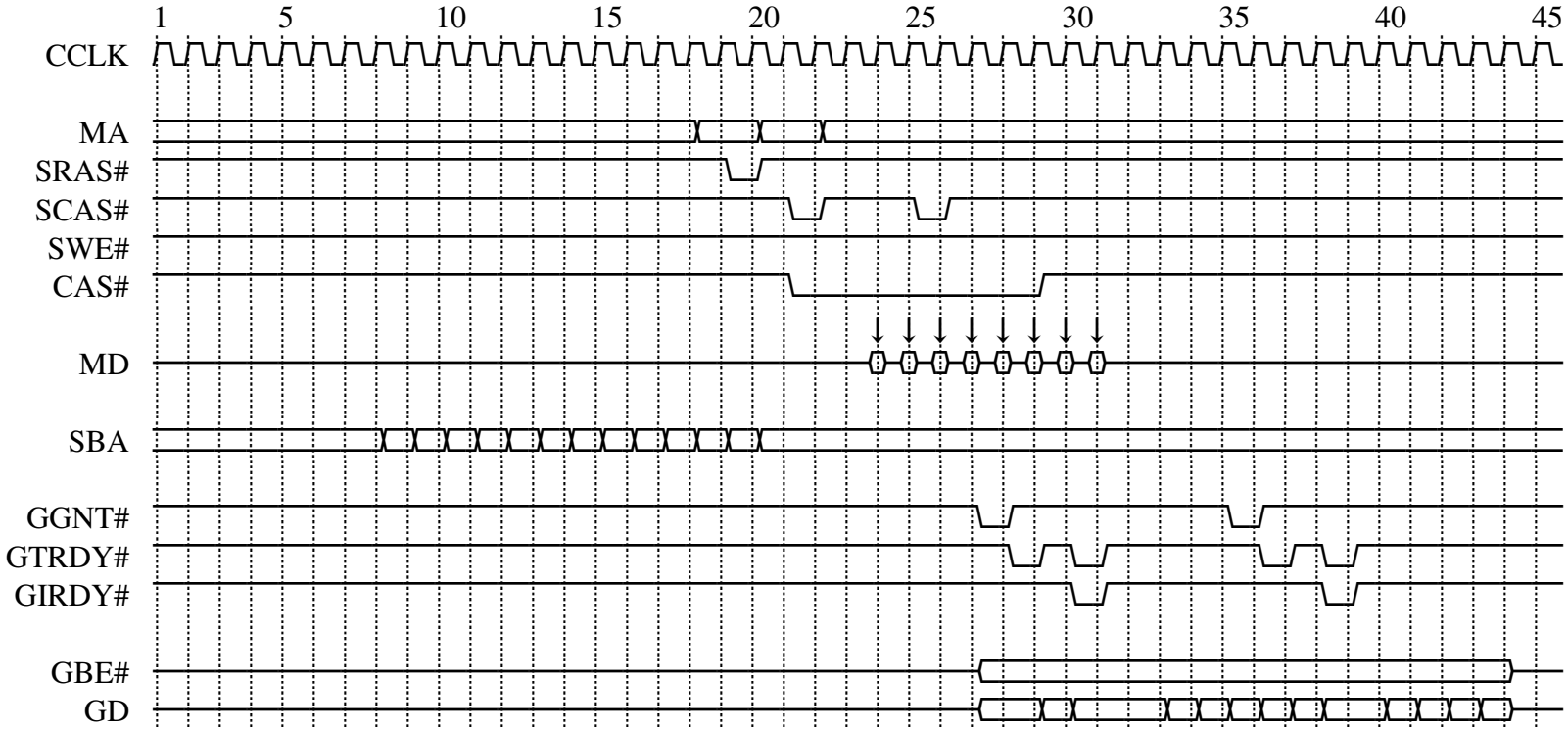


Figure 17. AGP Sideband Address 1x Read SDRAM (2L)

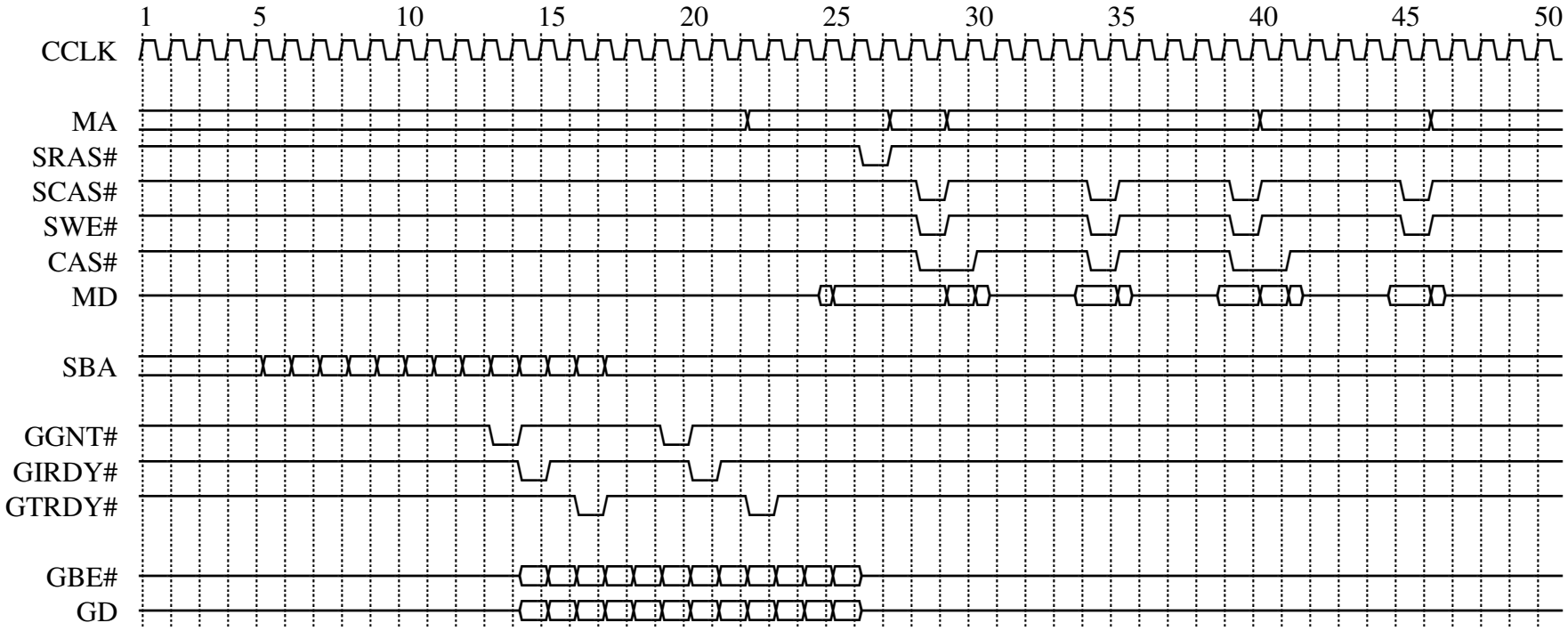


Figure 18. AGP Sideband Address 1x Write SDRAM

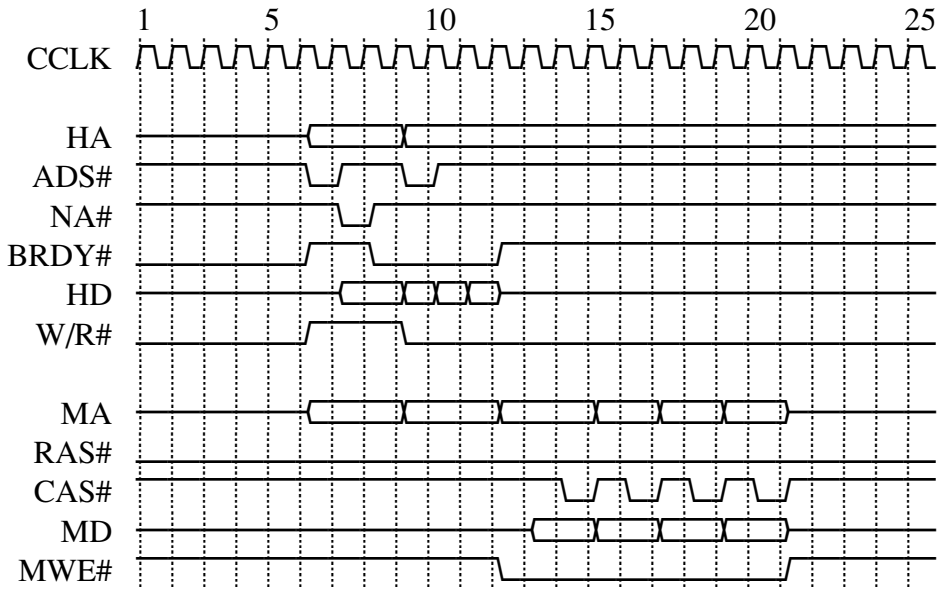


Figure 19. Post Write 3111, EDO DRAM 2222

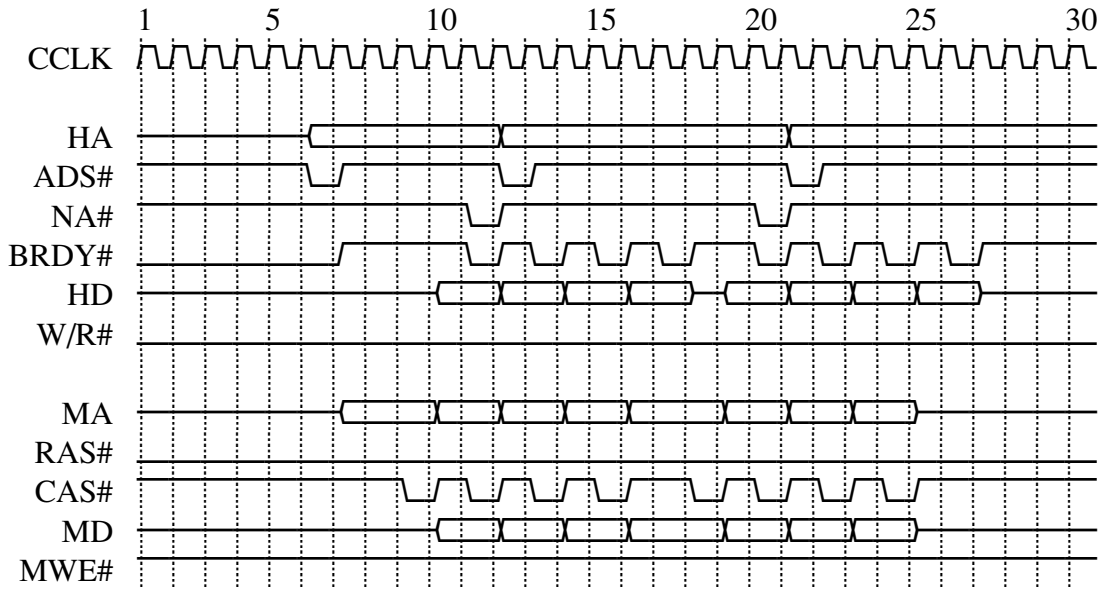


Figure 20. Pipeline Read EDO DRAM 6222, 3222

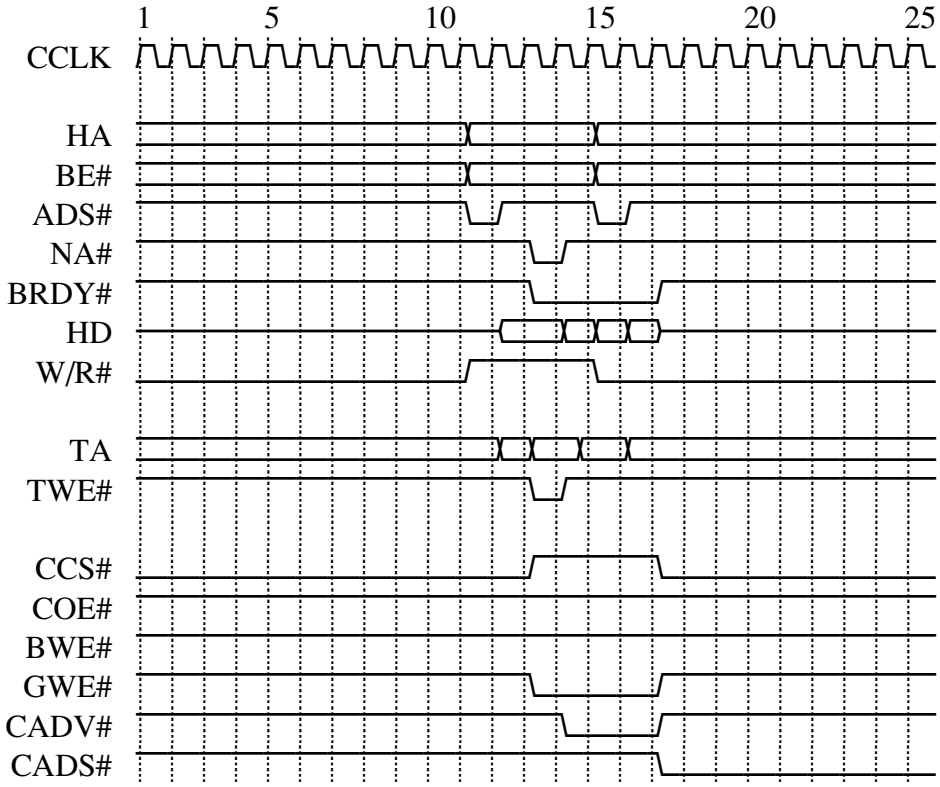


Figure 21. CPU Write Hit SRAM 3111

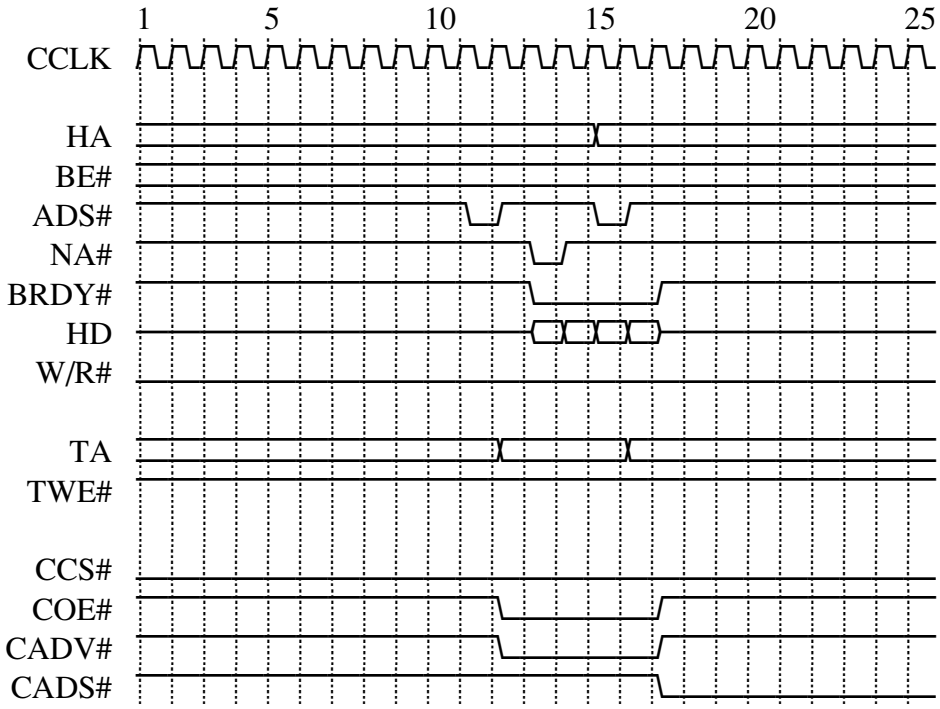


Figure 22. CPU Read Hit SRAM 3111

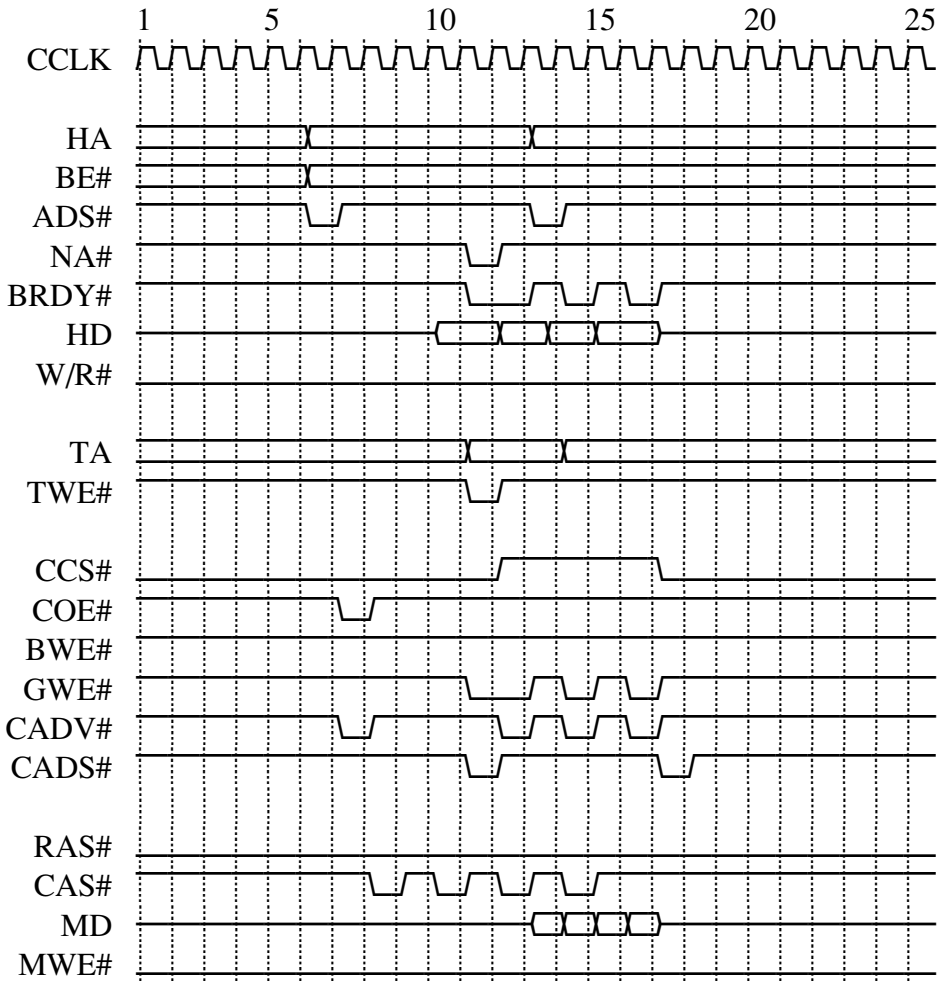


Figure 23. CPU Read Miss Fill Synchronous SRAM

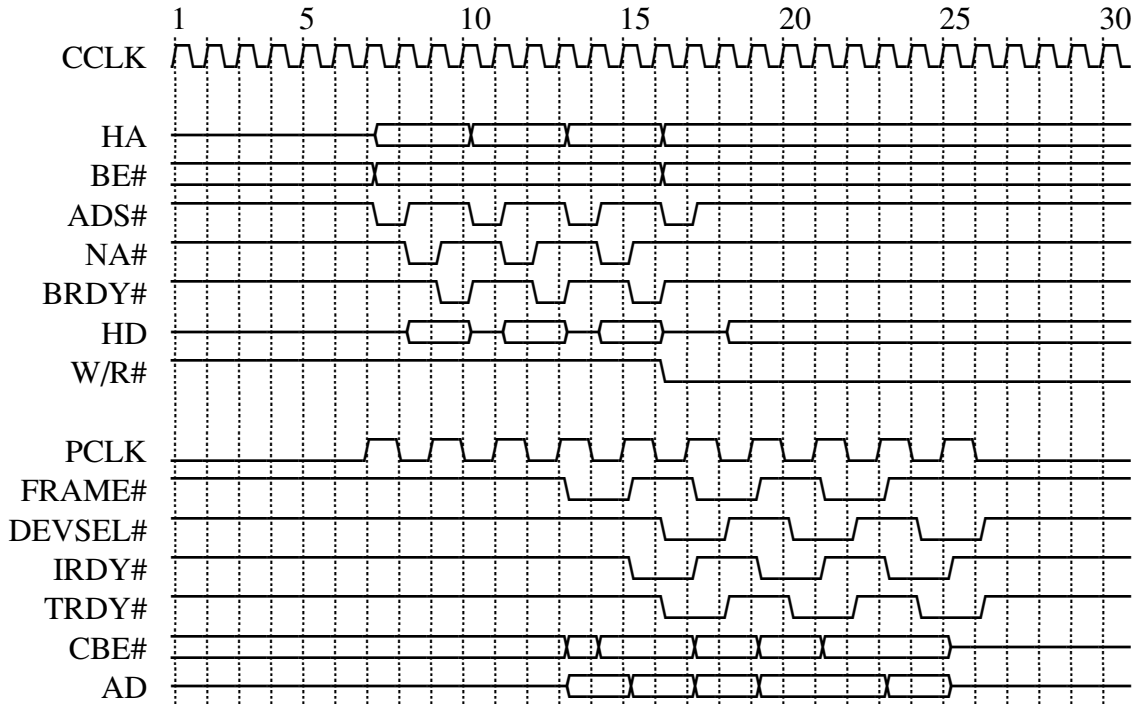


Figure 24. CPU Write PCI Slave Write Buffer on Fast Back-to-Back

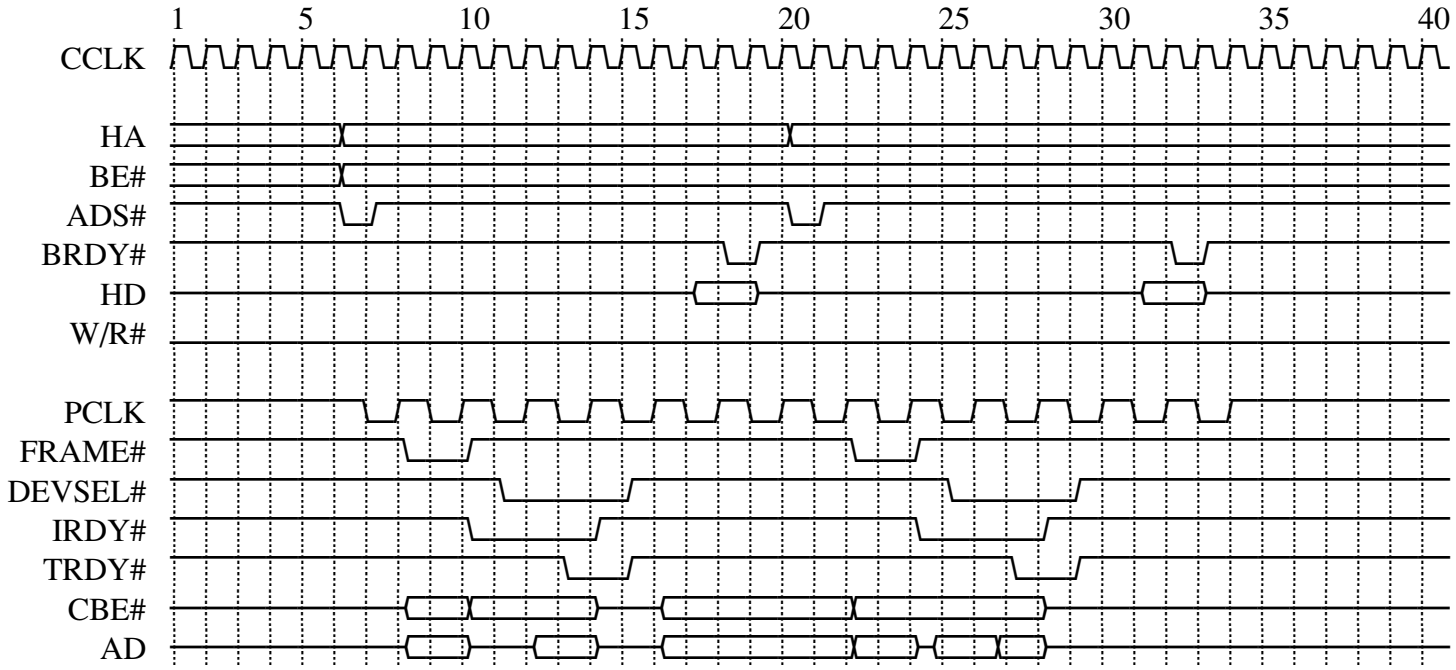


Figure 25. CPU Read PCI Slave

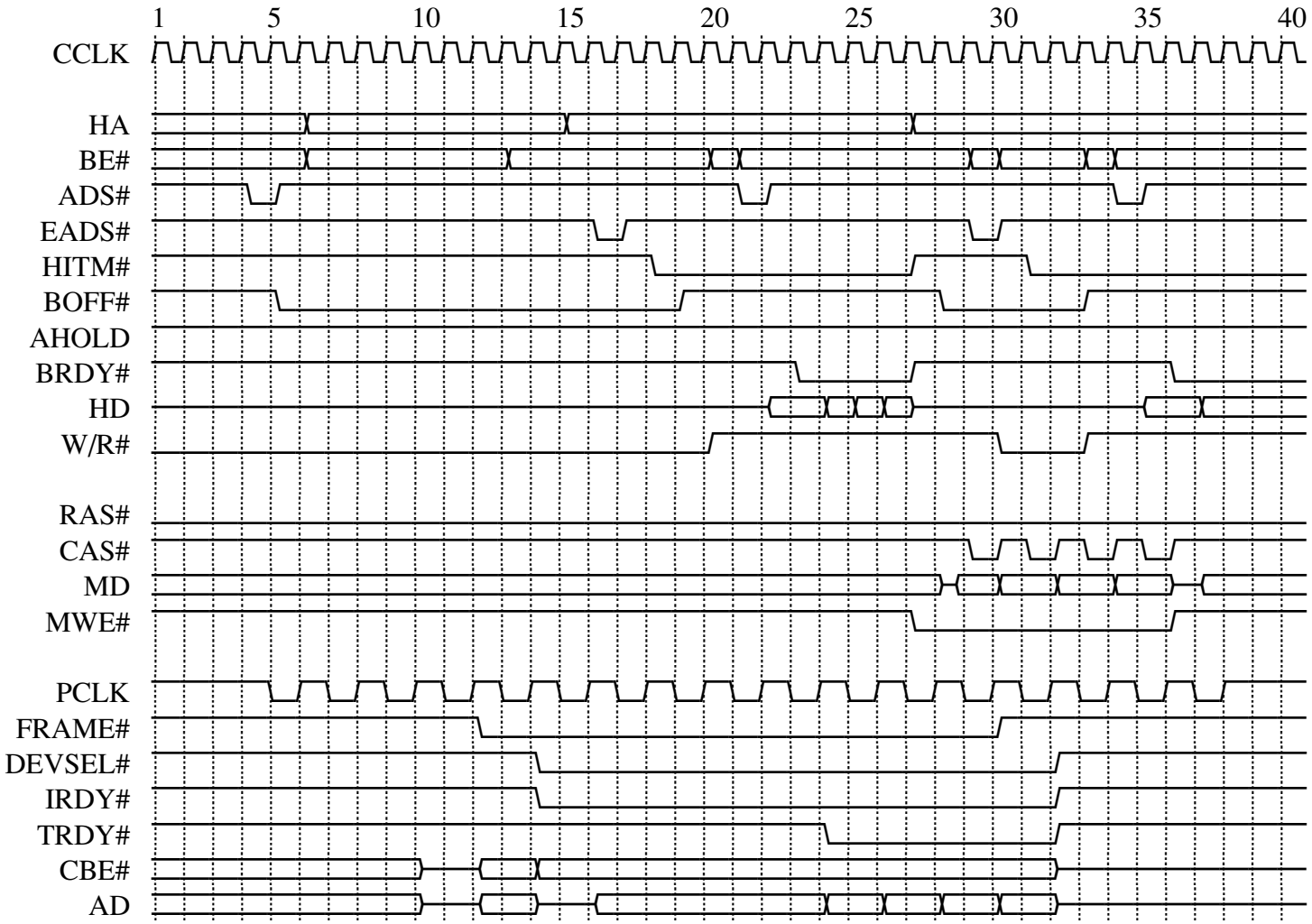


Figure 26. PCI Master Read L1 Snoop to DRAM

Figure 27. PCI Master Read Hit L2

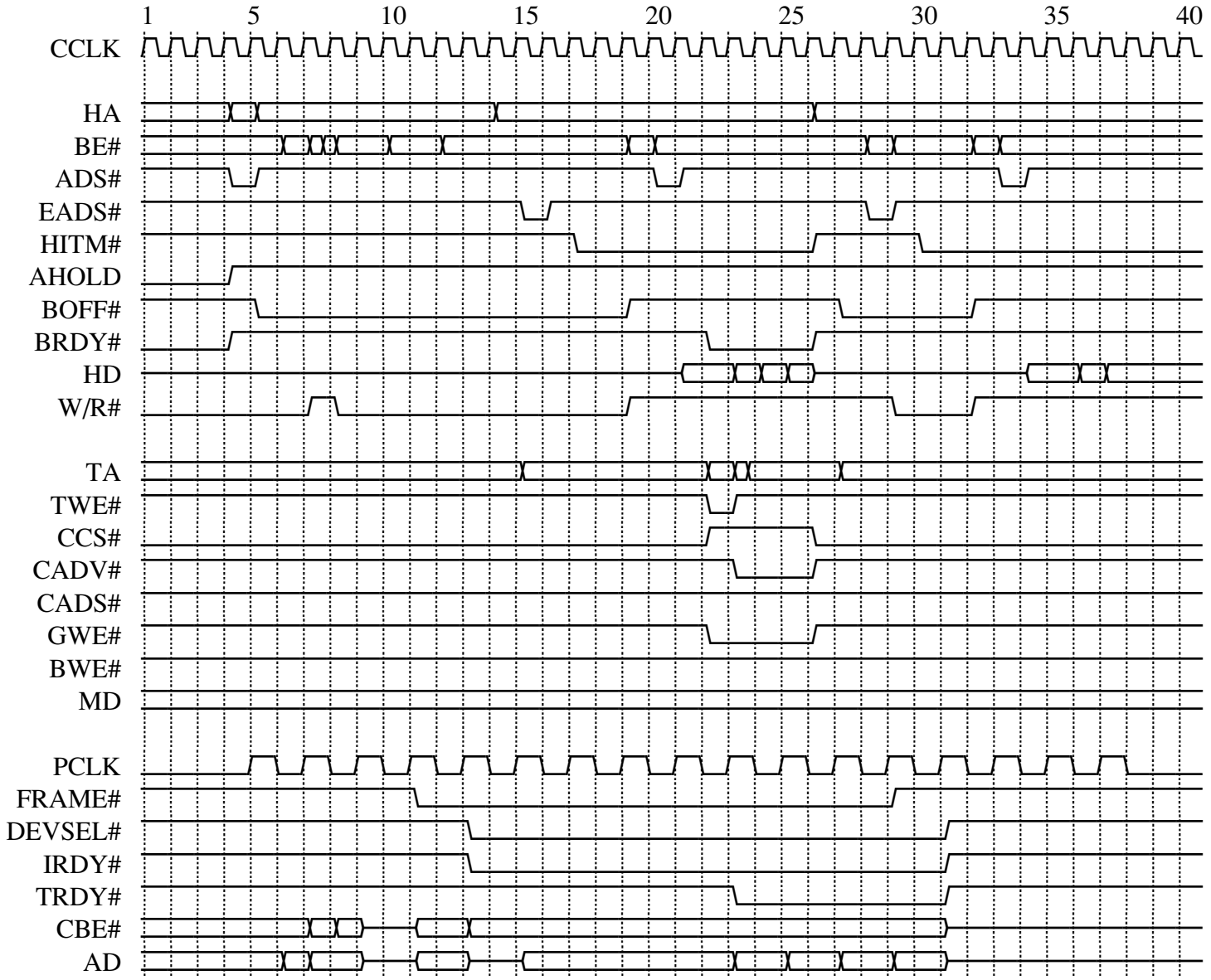


Figure 28. PCI Master Read L1 Snoop to L2

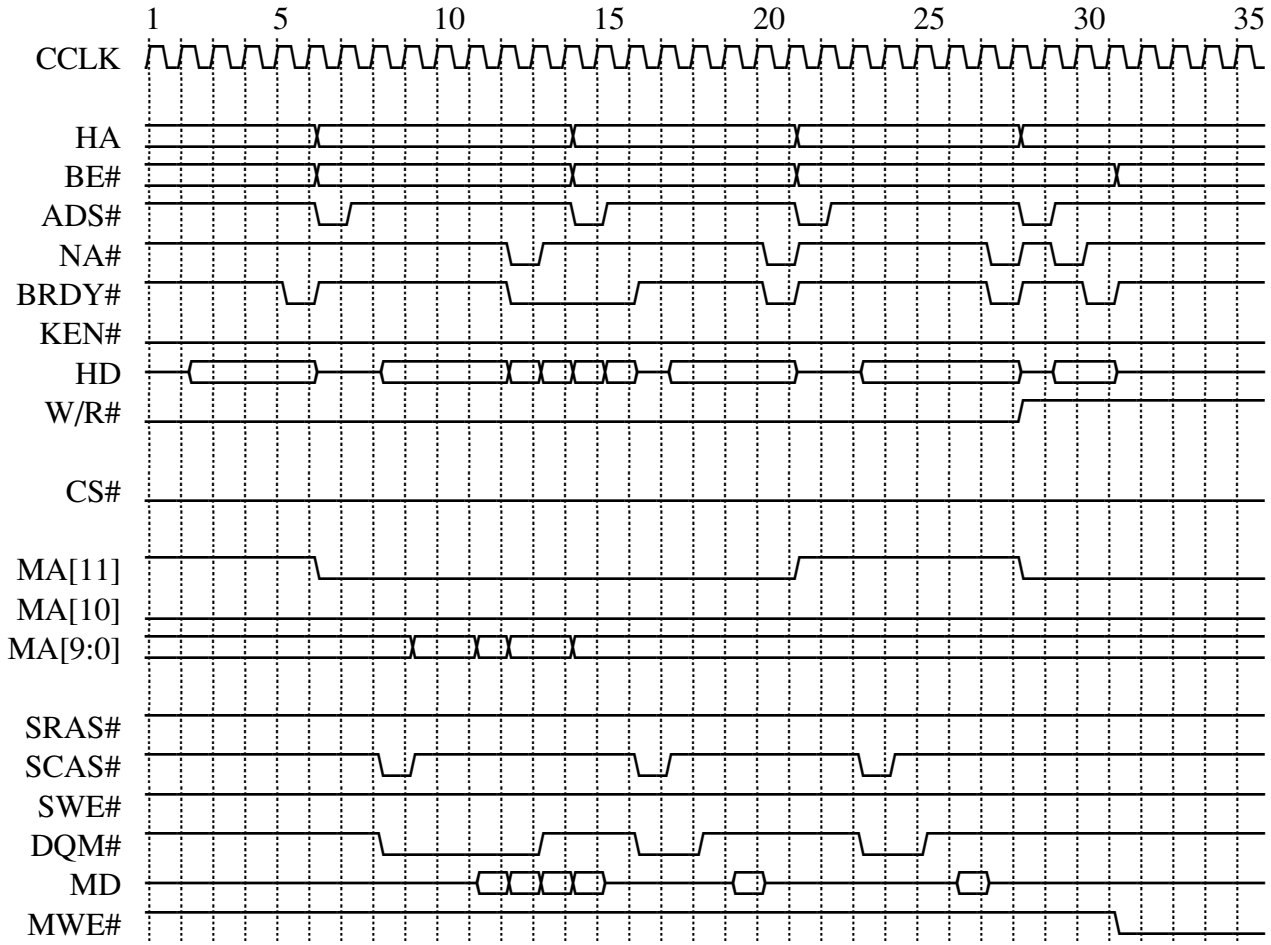


Figure 29. SDRAM Read Cycle (Bank Interleave, CAS Latency 3)

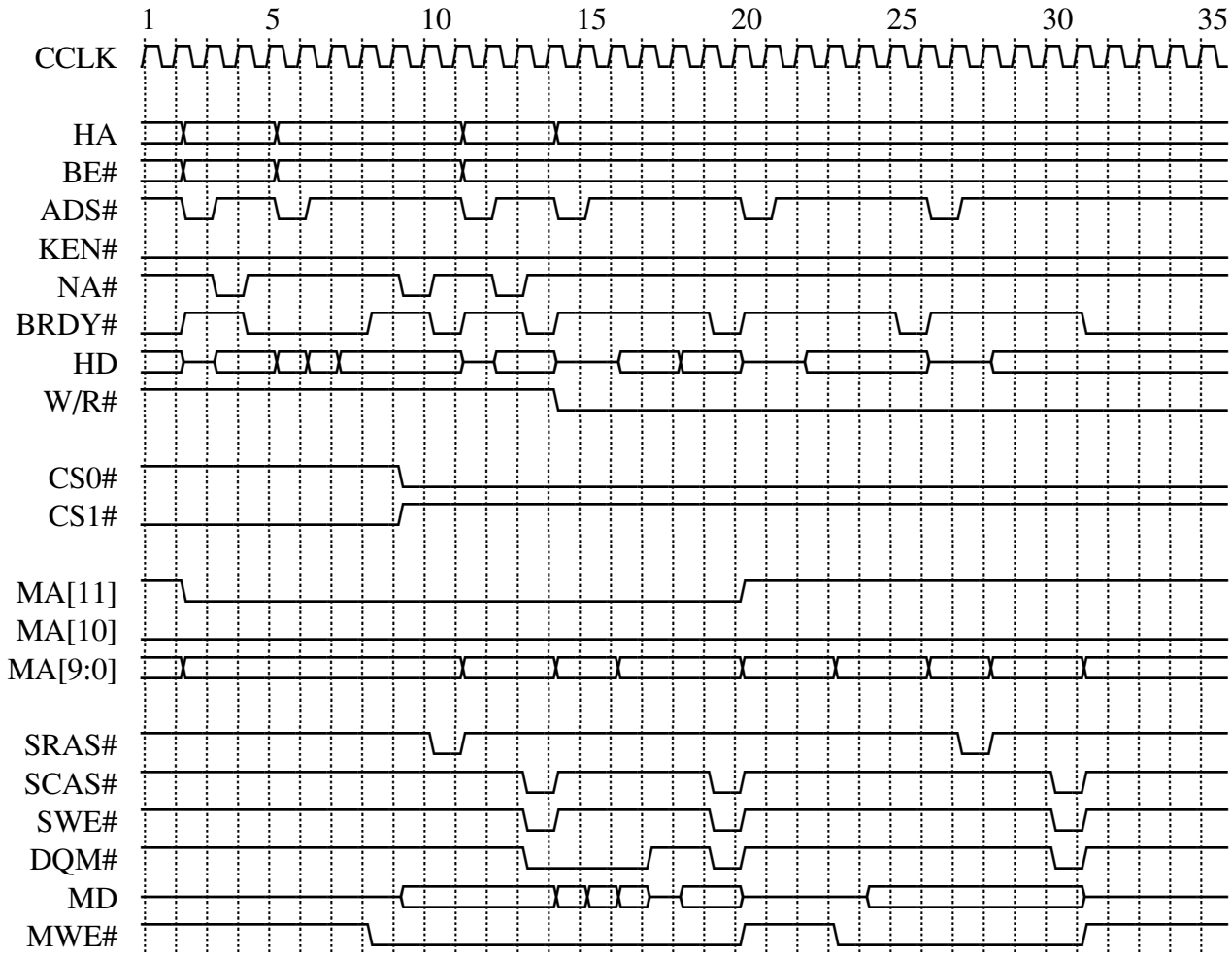


Figure 30. SDRAM Write Cycle (Bank Interleave)

Figure 31. PCI Master Read Hit DRAM

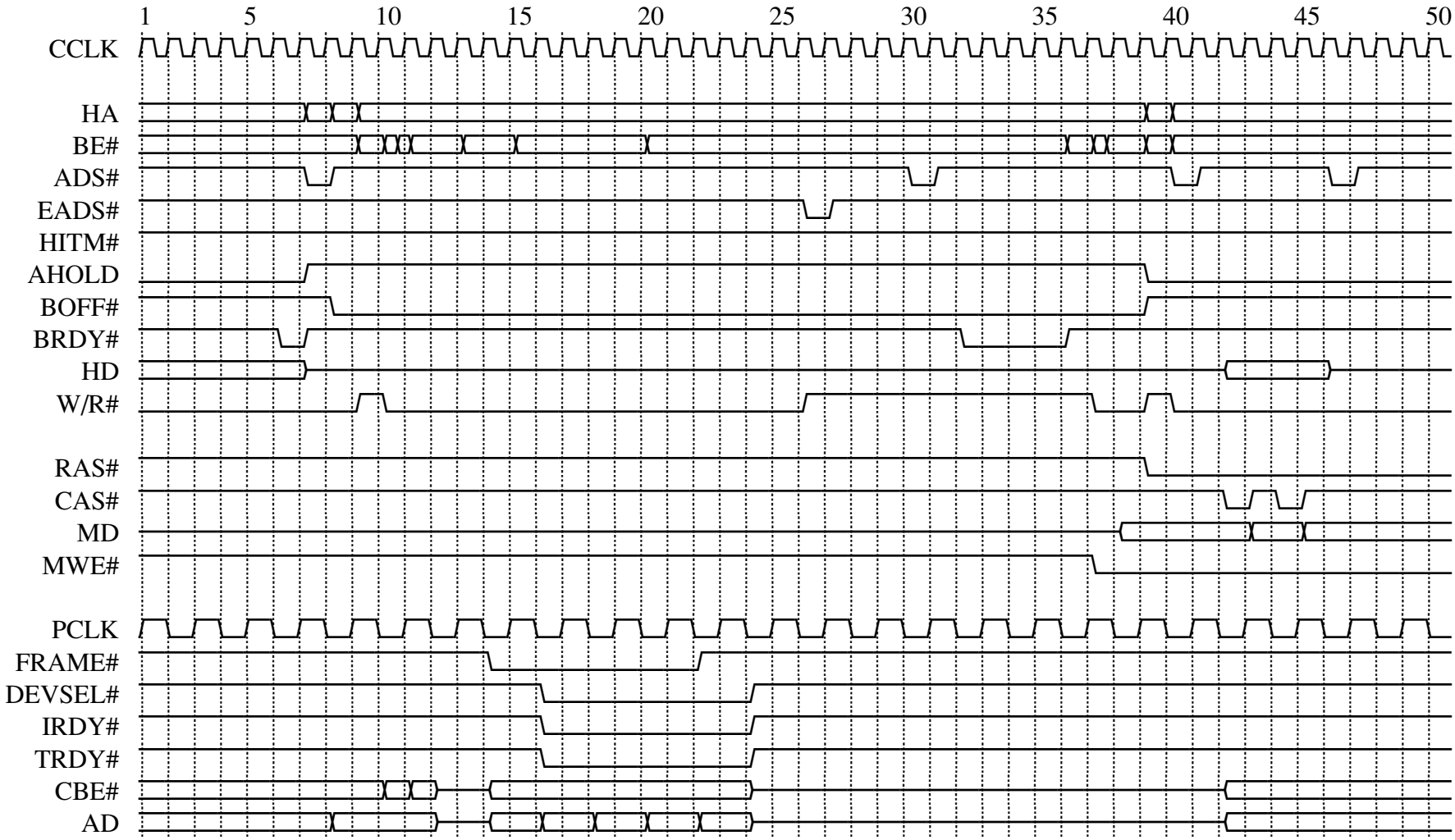


Figure 32. PCI Master Write DRAM

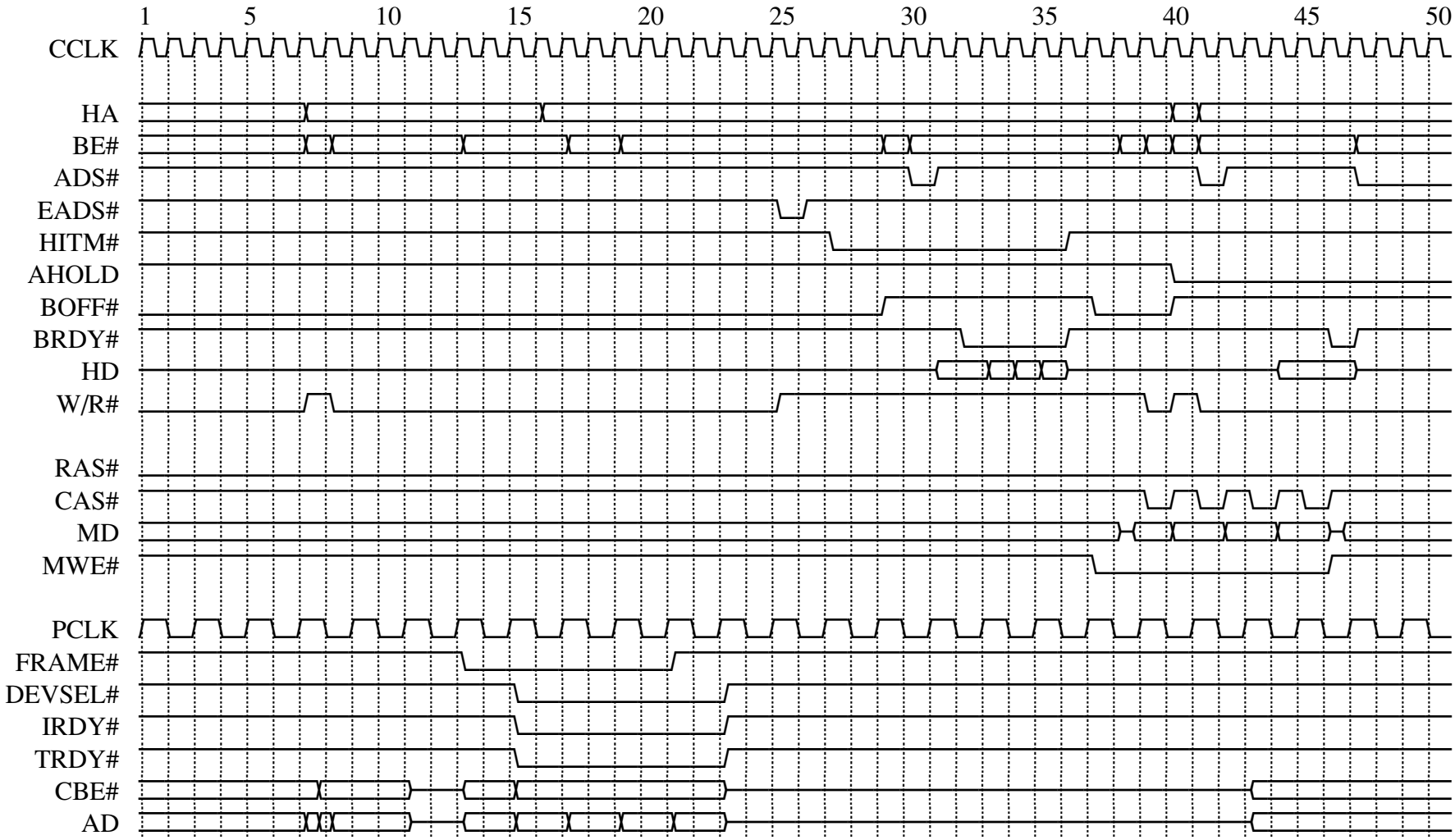


Figure 33. PCI Master Write Hit L1 Snoop to DRAM

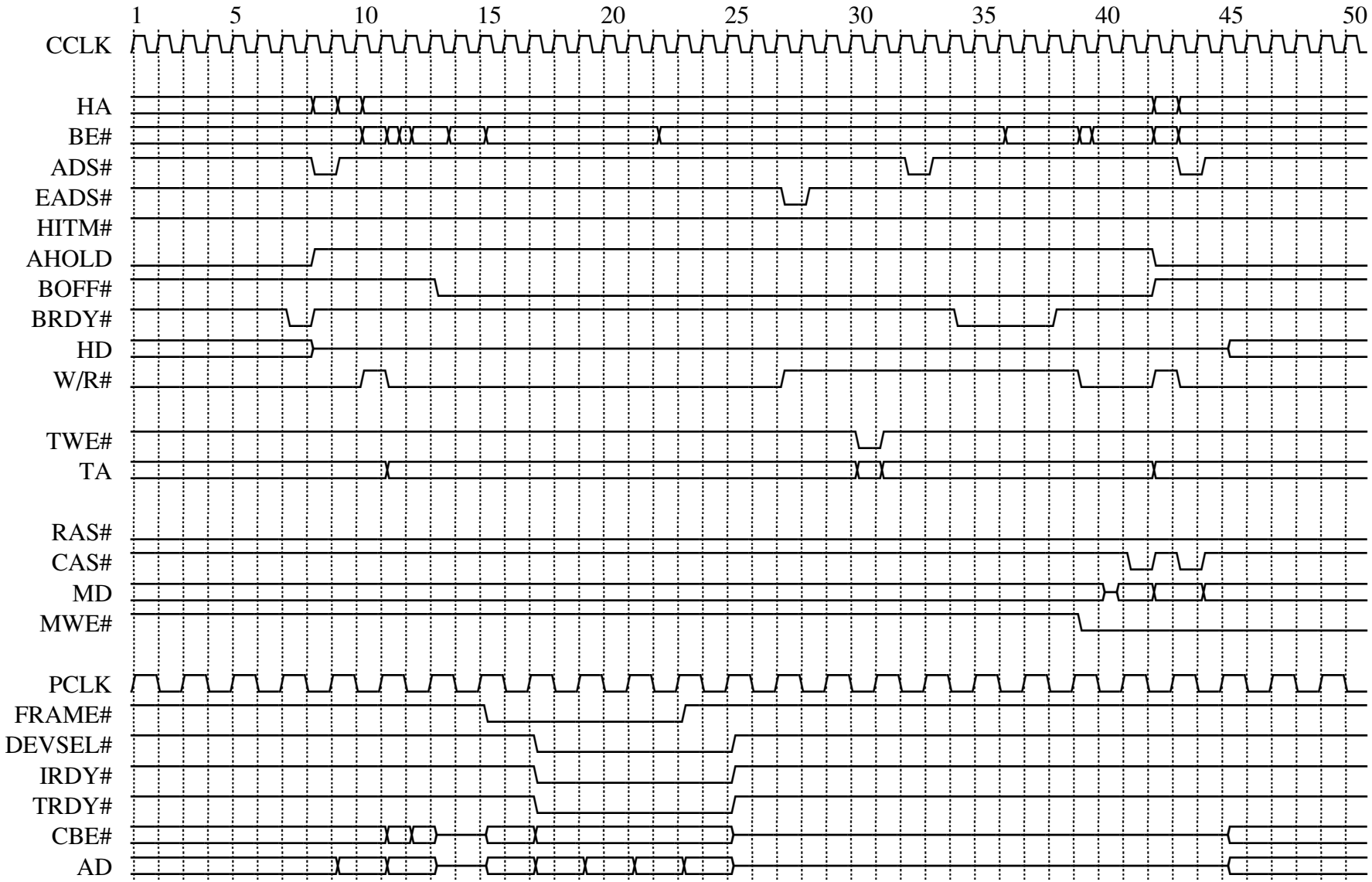


Figure 34. PCI Master Write Hit L2

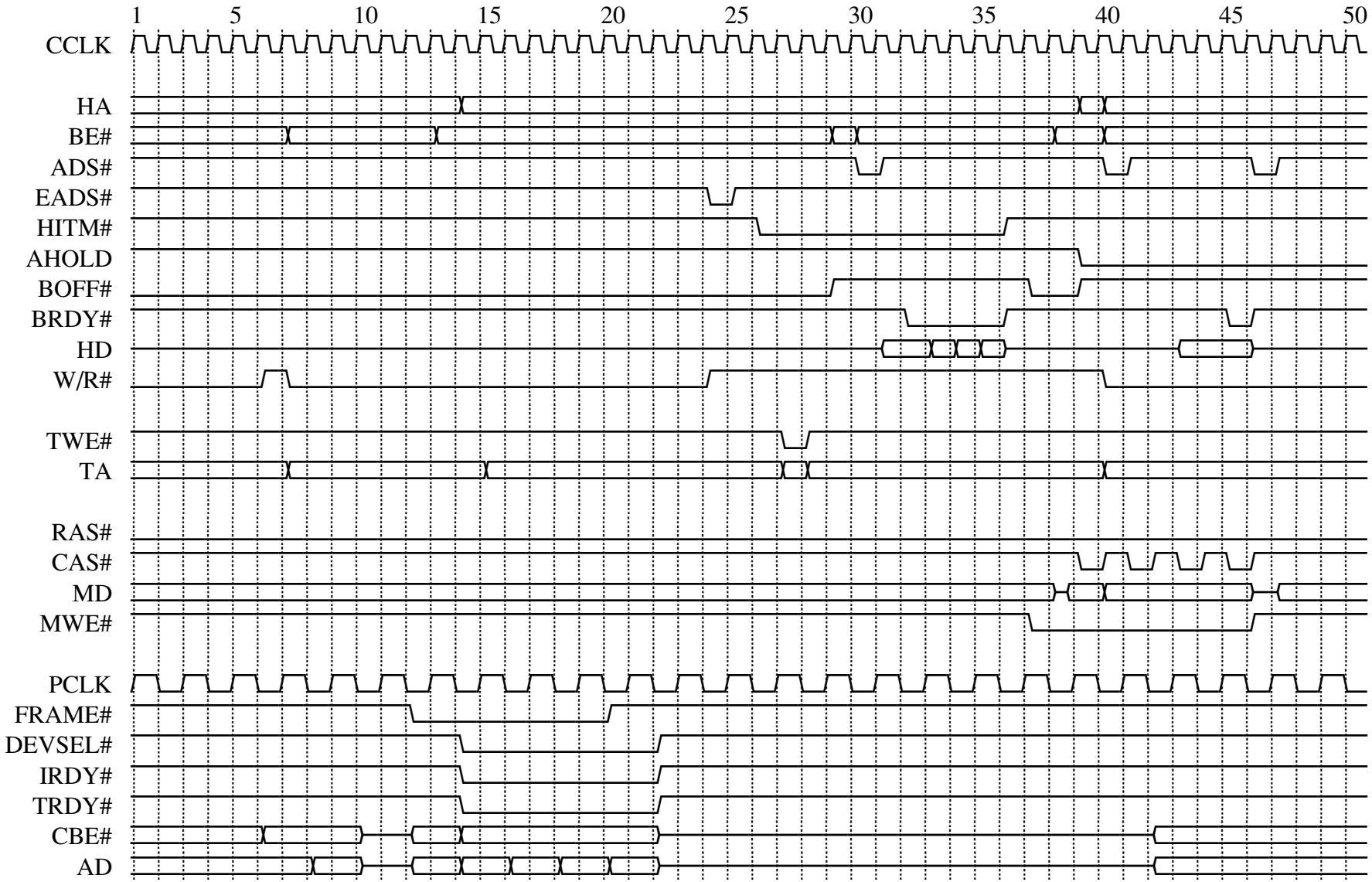


Figure 35. PCI Master Write Hit L2, L1 HITM

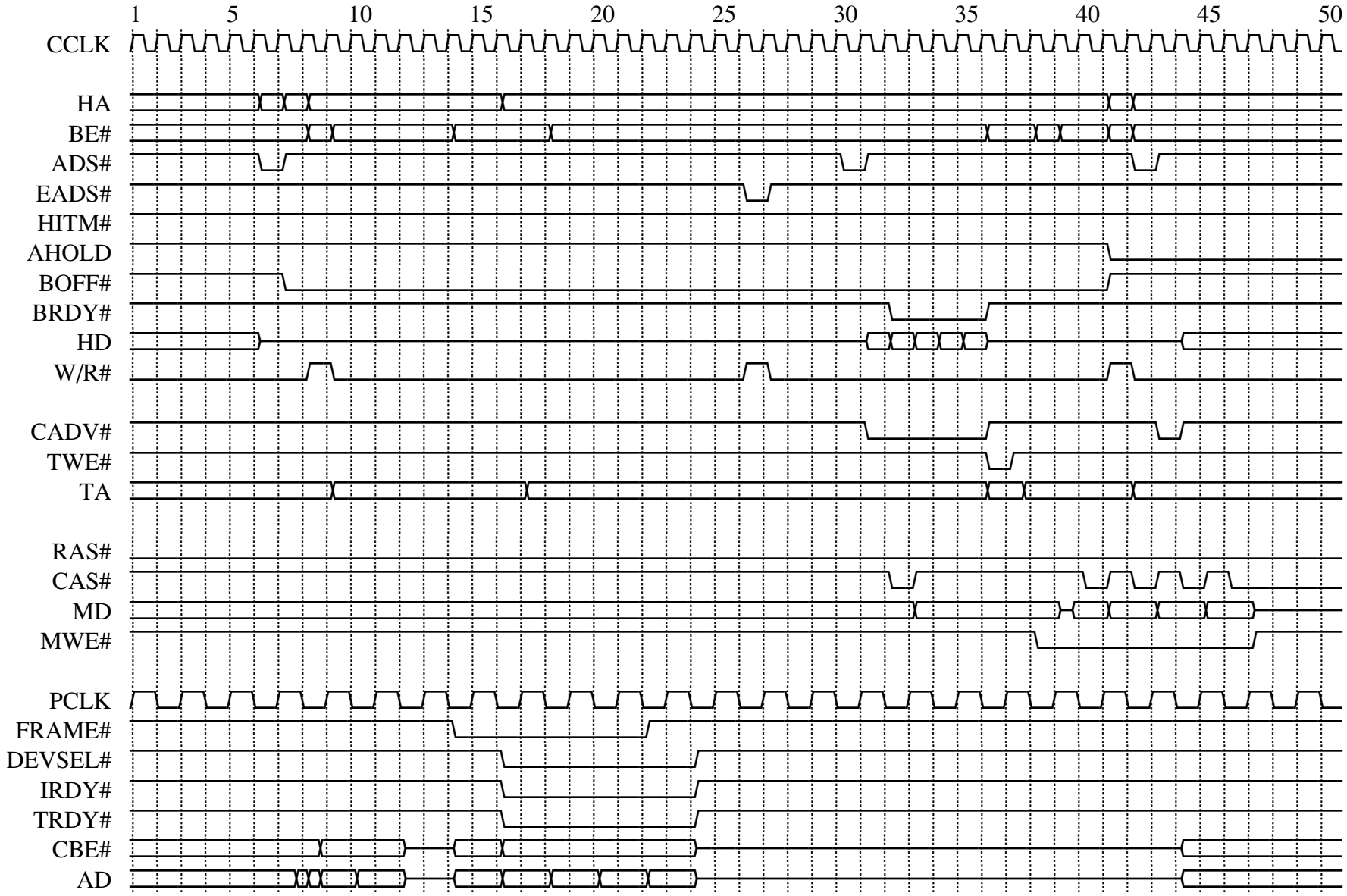


Figure 36. PCI Master Write Hit L2 & Dirty

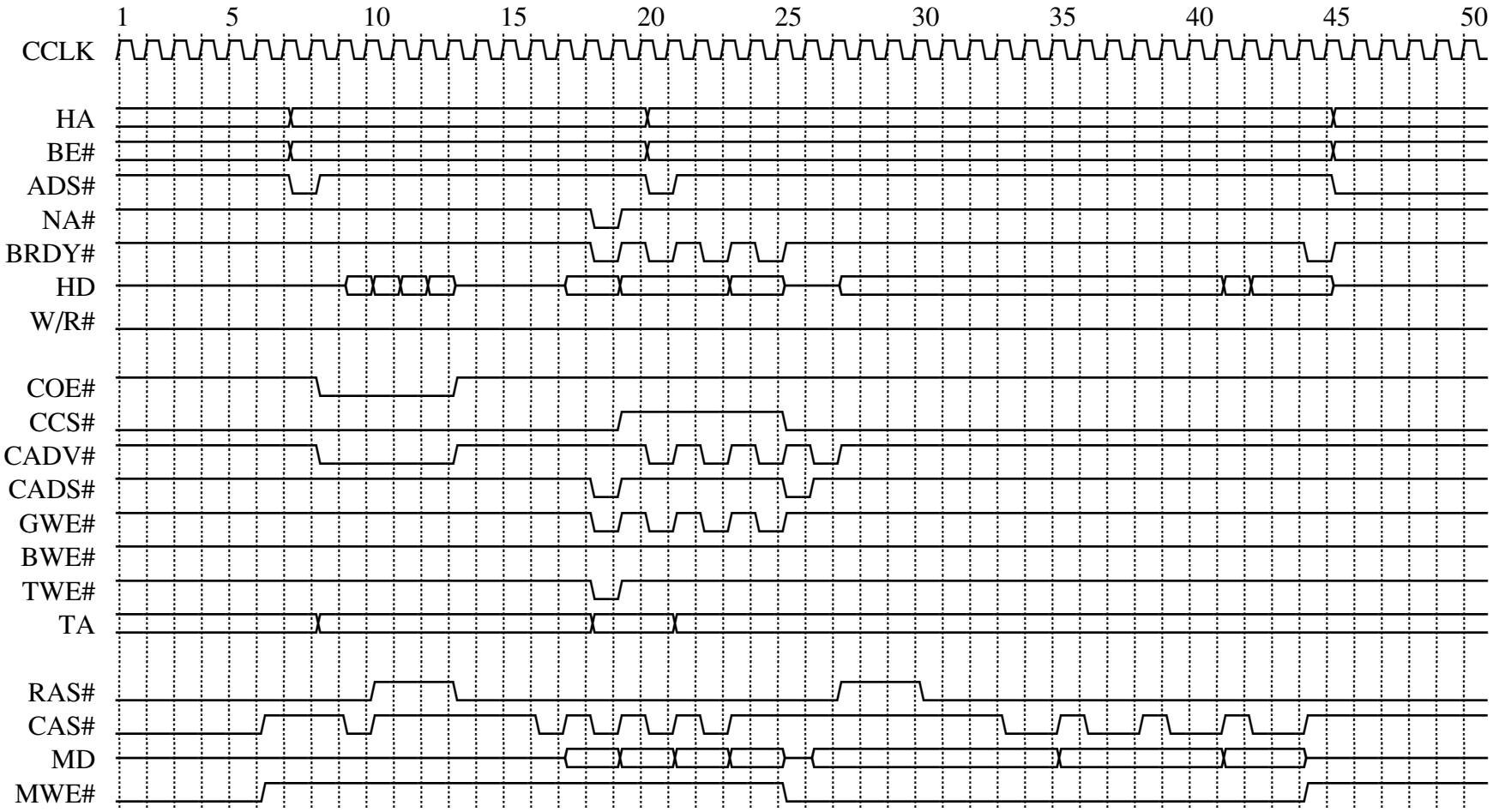


Figure 37. CPU Read Miss Dirty L2 Write Back Fill

MECHANICAL SPECIFICATIONS

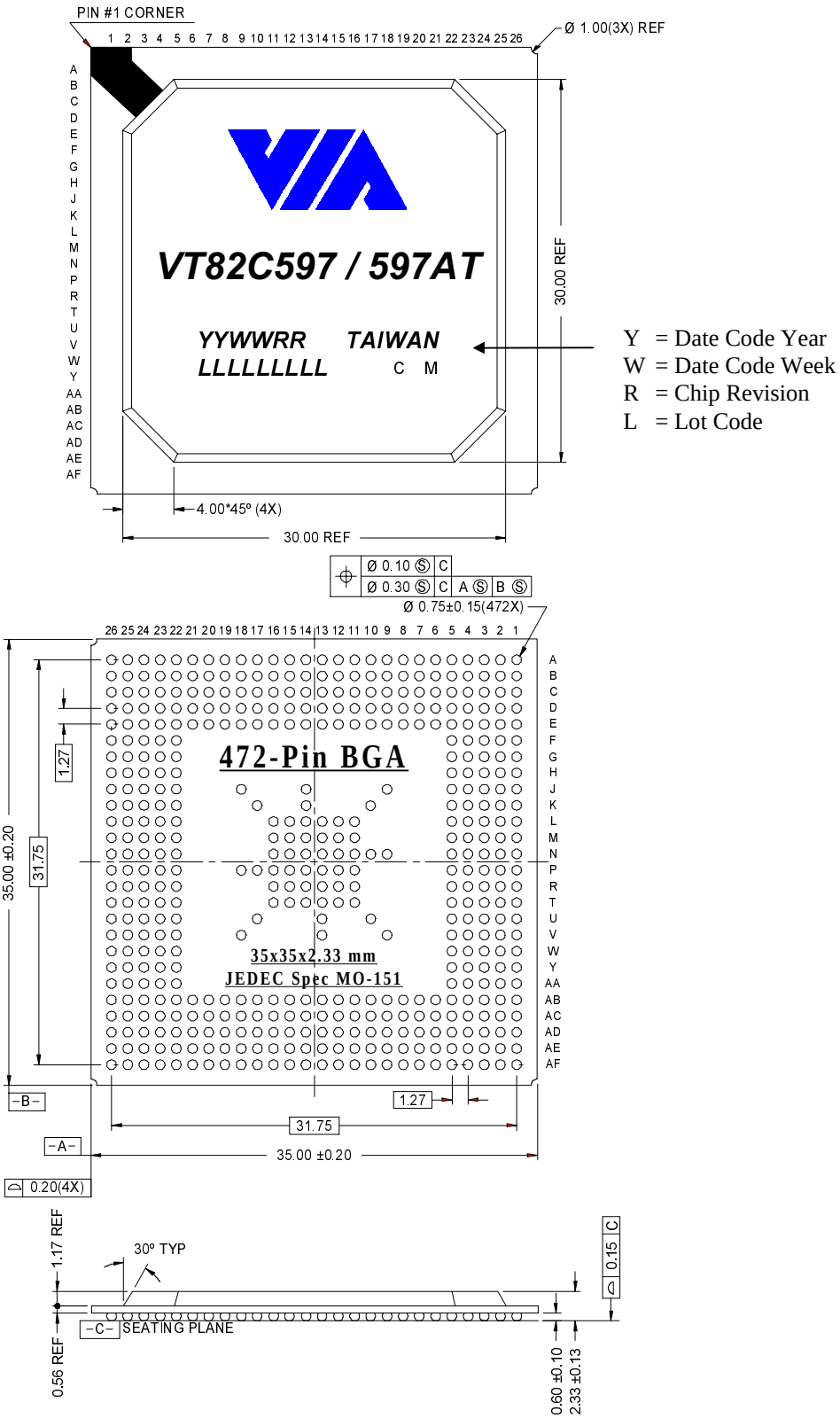


Figure 39. Mechanical Specifications - 472-Pin Ball Grid Array Package