82559 Printed Circuit Board (PCB) Design

Application Note (AP-399)

Revision 1.0

January 1999

Order Number: 739073-001

Revision History

Revision Date	Revision	Description
Jan. 1999	1.0	First Release

Contents

Figures

1.0 Introduction

This application note provides guidelines for the physical layout of a printed circuit board (PCB) design that makes use of the 82559 Ethernet Controller. This document applies to network interface card and LAN-on-motherboard (LOM) designs.

Fast Ethernet (100 Mbps) uses low voltage differential signaling and drives at least 100 meters of Category 5 (CAT 5) cable. The stringent requirements of the communications channel places additional burdens on the PCB designer. Placement, routing, impedance control, and thermal management have become important criteria in overall design.

1.1 References

The following documents provide additional reference material for 82559-based designs.

- 82559 Fast Ethernet Multifunction PCI/CardBus Controller Datasheet
- Intel Packaging Databook, 1998

1.2 Recommended Reading

- Amkor Technology, Inc. Applications Notes on Surface Mount Assembly of BGA Packages, January 1998.
- IPC. Implementation of Ball Grid Array and Other High Density Technology, J-STD-013.

2.0 Guidelines for Component Placement

Component placement can affect signal quality, emissions, and temperature of a board design. This section provides guidelines regarding component placement.

If LAN components are placed close together, stripline design becomes less of an issue. This includes the layout of the LAN support components such as the crystal, or oscillator, circuitry. Careful component placement can:

- decrease potential problems directly related to electromagnetic interference (EMI), which may cause failure of FCC and IEEE test specifications.
- simplify the task of routing traces. To some extent, component orientation also affects the complexity of trace routing. The objective is to minimize the number of turns and crossovers between traces.

Minimizing the amount of space required for the Ethernet interface is important because the interface competes for physical space on the motherboard, near the connector edge. As with most subsystems, the LAN circuitry needs to be close to the connector (for example, an RJ-45). Thus, it is imperative that designs be optimized to fit in a very small space.

2.1 Crystals and Oscillators

To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports. Crystals should also be kept away from the Ethernet magnetics module. The retaining straps of the crystal should be grounded to reduce the possibility of radiation from the crystal case. Crystals should lay flat against the PC board to provide better coupling of electromagnetic fields to the board.

2.2 Termination Resistors

The differential transmit signal pair (TDP/TDN) is terminated with a 100 Ω (1%) resistor, and the differential receive signal pair (RDP/RDN) is terminated with a 120 Ω (1%) resistor. These termination resistors should be placed as close to the PHY as possible. These resistors terminate the entire impedance seen at the termination source (for example, the PHY), including the wire impedance reflected through the transformer. Figure 1 depicts the placement of the termination resistors.

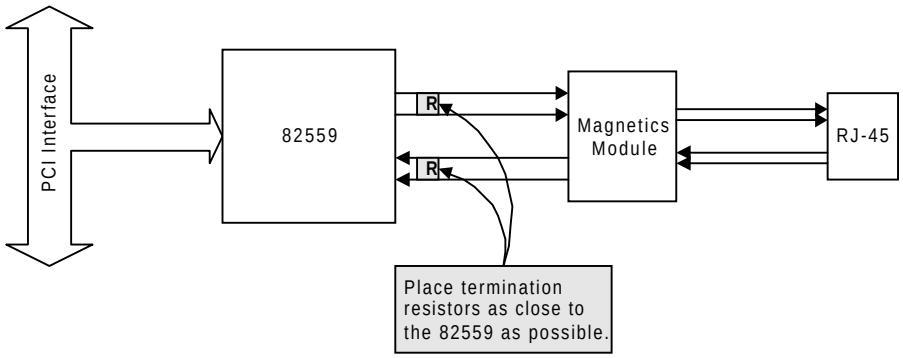


Figure 1. Placement of Termination Resistors

2.3 Critical Dimensions

There are two critical dimensions to consider during the layout phase of a board design. These dimensions are identified in Figure 2.

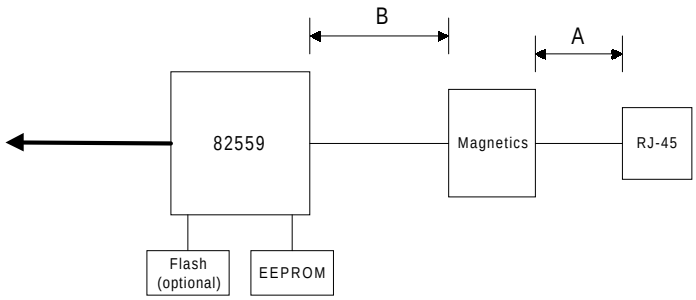


Figure 2. Critical Dimensions for Component Placement

2.3.1 Distance A: Magnetics to RJ-45 (Priority 1)

The distance between the magnetics module and the RJ-45 connector (labeled “A” in Figure 2) should be given the highest priority in board layout. This distance should be kept to less than one inch of separation. The following trace characteristics are important and should be observed:

- Differential Impedance: The differential impedance should be 100 Ω. The single ended trace impedance will be approximately 50 Ω; however, the differential impedance can also be affected by the spacing between the traces.
- Trace Symmetry: Route differential pairs (such as TDP and TDN) with consistent separation and with exactly the same lengths and physical dimensions (for example, width).

Caution: Asymmetrical and unequal length traces in the differential pairs contribute to common mode noise. This can degrade the receive circuit performance and contribute to radiated emissions from the transmit circuit. If the PHY must be placed more than a couple of inches from the RJ-45 connector, distance B identified in Figure 2 can be sacrificed. Keeping distance A as short as possible is the priority.

2.3.2 Distance B: PHY to Magnetics (Priority 2)

Due to the high-speed of signals present, distance B in Figure 2 should be designed to extend less than one inch between devices. In general, any section of trace that is intended for use with high-speed signals should observe proper termination practices.

Proper signal termination can reduce reflections caused by impedance mismatches between device and traces. The reflections of a signal may have a high-frequency component that may contribute more EMI than the original signal itself. For this reason, these traces should be designed to a 100 Ω differential value.

3.0 General Trace Routing Considerations

Trace routing considerations are important to minimize the effects of cross-talk and propagation delays on sections of the board where high speed signals exist.

This section provides general as well as 82559-specific trace routing guidelines. Examples from Appendix A, “82559 Layout Diagrams” in this document are used to illustrate specific routing results. Depending on the design for manufacturing rules used, an appropriate keep-out zone around the BGA is required for rework purposes. The requirements for the keep-out zone is determined by the type of rework equipment used. The example provided is a four-layer design with the signal run on the top and bottom layers. The power planes are internal to the stack. Figure 3 shows the layer stack used in this example.

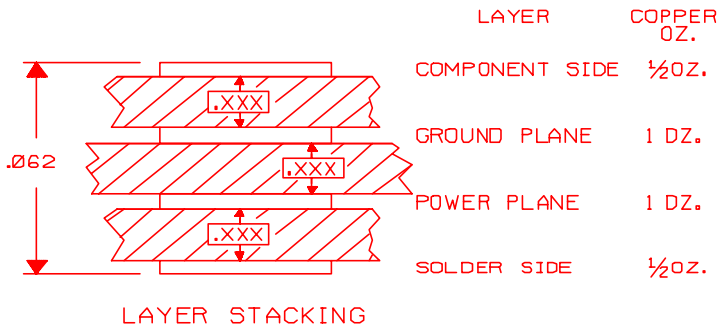


Figure 3. Printed Working Assembly Layer Stack

3.1 Trace Routing

Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes. Capacitive loading, which is caused by the signal trace, can also be reduced by keeping the traces as short as possible.

Note: Observe the following suggestions to help optimize subsystem and board performance:

- The maximum separation distance between differential pairs should not exceed one tenth of an inch. However, it is more important to keep the signal trace lengths equal to each other than to observe the one tenth of an inch separation throughout the route.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90^{o} turn is required, use two 45^{o} bends instead.
- Traces traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires, boards, etc.
- Routing traces and vias under crystals or oscillators should be avoided to reduce the coupling area.

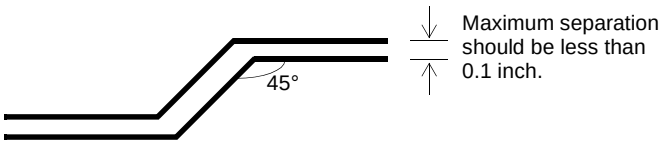
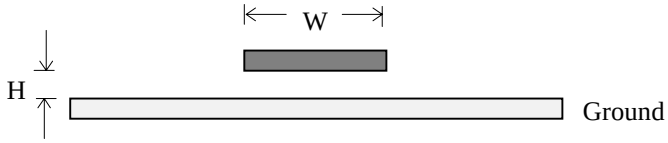


Figure 4. Trace Routing

As a general rule, traces from clocks and drivers should be placed at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

3.2 Trace Geometry

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals, such as the clock, and signal layers that are close to a ground plane or power plane should be as short and as wide as is practical. As shown in Figure 5, this ratio is ideally somewhere between 1:1 and 3:1.



$$\frac{1}{1} < \frac{W}{H} < \frac{3}{1}$$

W = Trace Width
H = Height Above Ground Plane

Figure 5. Trace Geometry

To maintain the impedance of a trace, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from a power or ground plane.

3.3 Trace Length

The traces between decoupling and I/O filter capacitors should be short and as wide as is practical. Long and thin traces are more inductive and reduce the effectiveness of the decoupling capacitors. For similar reasons, traces to I/O signals and terminations should be as short as possible. Also, plated vias to the decoupling capacitors should be larger in diameter to decrease series inductance.

3.4 Signal Isolation

Signals should be separated and grouped by function on separate layers if possible. Physically grouping together all components associated with one clock trace can reduce the trace length and radiation. Isolate I/O signals from high speed signals to minimize cross-talk. Cross-talk can increase both emission and susceptibility to EMI from other signals. Avoid routing high-speed LAN traces near other high-frequency signals associated with video controller, cache controller, and CPU, and other similar devices

3.5 Power and Ground Connections

All V_{CC} pins should be connected to the same power supply, and all V_{SS} pins to the same ground plane of the 82559. For main power and V_{CC} decoupling, the number of capacitors used in the design may be reduced at the designer's discretion. For optimized performance, decoupling capacitors should be placed as close to the 82559 as possible. Optimal performance can be achieved by placing decoupling capacitors on the backside of the circuit board directly under the 82559. Four to six decoupling capacitors, including two 4.7 µF capacitors, will help improve performance.

4.0 General Power and Ground Plane Considerations

To properly implement the common mode choke functionality of certain magnetics module (such as Pulse Engineering's H1012) the input ground plane must be separated from the output ground plane by either a physical separation or a void under either section. Good grounding requires taking precautions to minimize inductance levels in the interconnections. Keeping ground returns short, signal loop areas small, and power inputs bypassed to the signal return, will significantly reduce radiation levels. See Figure 6 on page 6.

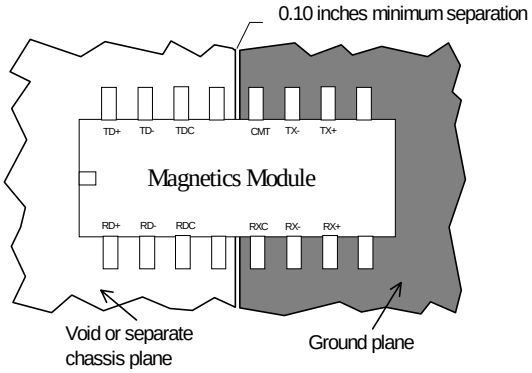


Figure 6. Ground and Power Connections for the Magnetics Module

Use the following guidelines to help reduce circuit inductance in both back planes and motherboards.

- Route traces over a continuous ground plane with no interruptions. If there are vacant areas on a ground or power plane, avoid routing signal conductors over the vacant area; routing signals over such areas increases inductance and radiation levels.
- Separate noisy logic grounds from analog signal grounds to reduce coupling. Noisy logic grounds can sometimes affect sensitive DC subsystems such as analog to digital conversion, operational amplifiers, etc. All ground vias should be connected to every ground plane and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance. Physically locate grounds to minimize the loop area between a signal path and its return path.
- Rise and fall times should be as slow as possible. Signals with fast rise and fall times contain many high-frequency harmonics which can radiate significantly.

- The most sensitive signal returns closest to the chassis ground should be connected together. This will result in a smaller loop area and reduce the likelihood of cross-talk. The effect of different configurations on the amount of cross-talk can be studied using electronics modeling software.

5.0 Terminating Unused Connections

For Ethernet designs, it is common practice to terminate unused connections on the RJ-45 connector and the magnetics line interface module to ground. Depending on the overall shielding and grounding design, this may be done to the chassis ground, signal ground, or termination plane. Care must be taken when using various grounding methods to insure that emission requirements are met.

The method most often implemented is called the “Bob Smith” termination. This method uses a floating termination plane that is cut out of a power plane. The floating plane acts as a capacitance plate with the adjacent plane. The signals can be routed through 75 Ω resistors to the plane and stray energy on unused pins are dumped to the plane.

The termination plane capacitance should equal a minimum value of 1500 pF. This helps reduce the amount of cross-talk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ-45. Pads may be placed for an additional capacitance to chassis ground, which may be required due to failure of electrical fast transient testing. See Figure 6.

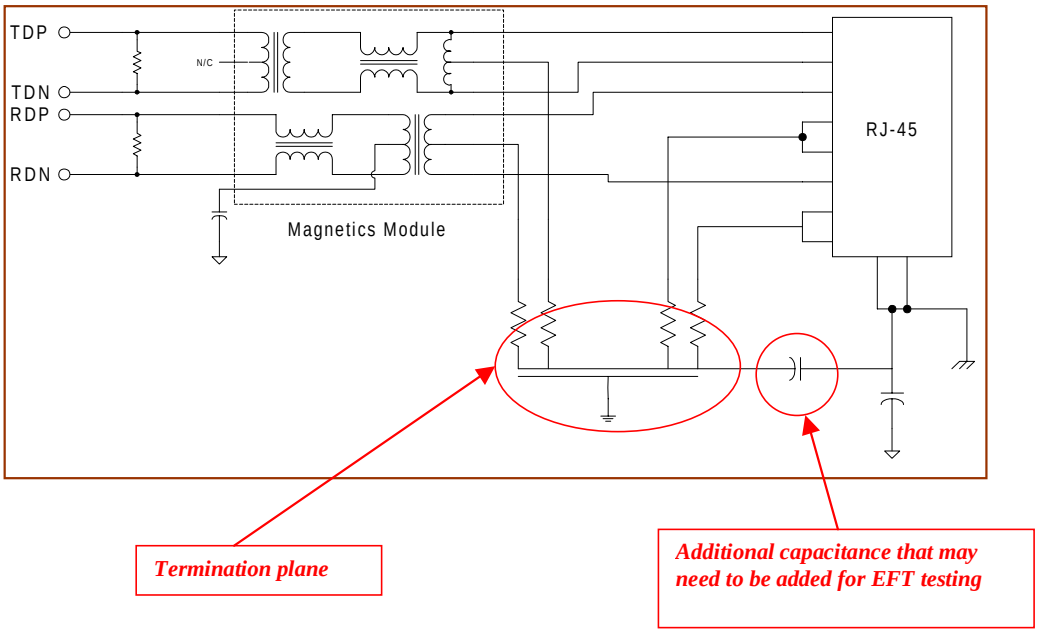
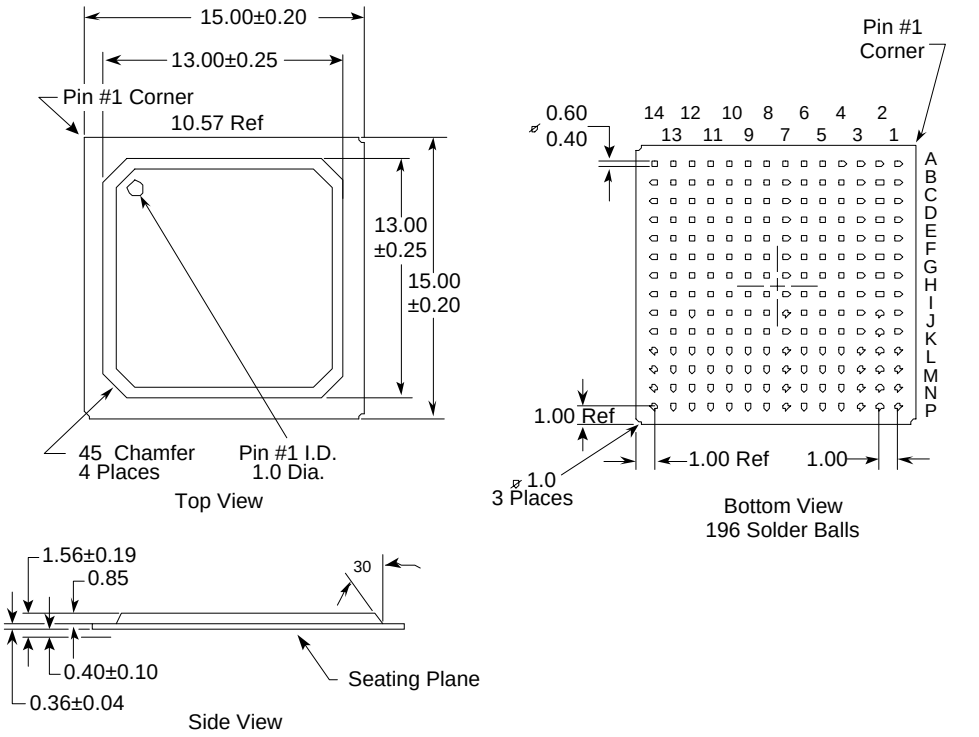


Figure 7. Terminating Unused Connections on the RJ-45 Connector

6.0 196-pin Ball Grid Array

The 196-pin Ball Grid Array (BGA) packaging was chosen for the 82559 to provide the highest-performance package. The 196 BGA enables the 82559 to provide a smaller footprint to reduce the impact of LAN-on-motherboard designs. The result is a considerably smaller finished design size with shorter electrical path lengths. The thin profile and smaller footprint make the 82559 an attractive option when board space is a major concern, such as CardBus and LAN-on-notebook designs.

The mechanical dimensions for the 15 mm^2 package is shown in Figure 8.



NOTE: All dimensions are in millimeters.

Figure 8. 196-pin Ball Grade Array Mechanical Specifications

7.0 Designing Boards for the 196-pin BGA

Optimization for manufacturing yields is one of the greatest challenges for designers using ball grid array packaging. Take care when selecting a pad criteria. Your printed circuit board supplier should be able to consult with you on the methodology that is most appropriate. As a general rule, most BGA packages use Solder Mask Defined (SMD) pads. PCB pad size will usually track close to the package pad size to balance stresses during thermal cycling. Additional manufacturing trade-offs may be required.

Designing for manufacturability is a critical consideration in maximizing yields using the 82559's 196-pin BGA package. The assembly process heavily relies on the design of the surface mount pads. Pad design methods that meet the needs of larger package types may not meet the requirements of a BGA package. Overall, the design requires an array of round pads to provide the mounting surface.

At first glance, the easiest method is to use the mounting pads that contain the vias. Unfortunately, the mounting pads must be isolated from any vias plated through holes (PTHs). This prevents the solder balls from leeching into the vias. Therefore, a connection from the PTH interstitial to the mounting pads is used.

Dimensional control of the pad is critical to achieving high yields in assembly. The designer will need to perform a comparison of the two methods, Solder Mask Defined (SMD) and Non-SMD (or copper defined), for the purpose of delimiting the pad area. Non-SMD is most commonly used in circuit design prior to the advent of BGA packaging. See Figure 9

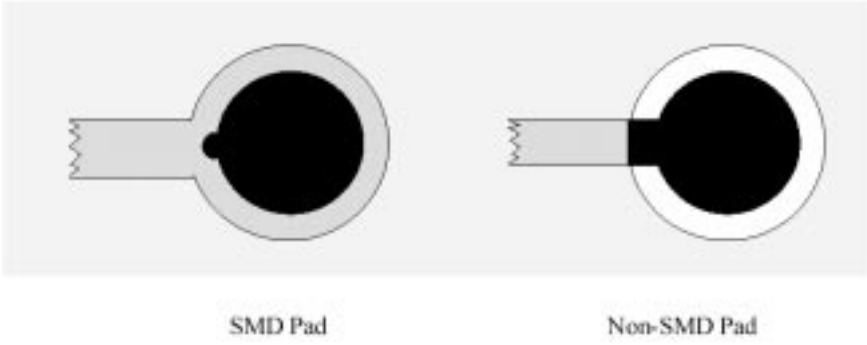


Figure 9. Pad Delimitation Options

7.1 Solder Mask Defined (SMD) Pad

The SMD pad method uses the solder mask to define the usable pad. The copper for the pad area is usually larger than the desired solderable area. The solder mask provides a smaller opening diameter which limits the usable area to the desired size. The advantages to this method are:

- The solder mask is a photographically controlled instead of being at the mercy of the etch process.
- The solder mask enhances copper adhesion by lying over the top of the pad surface.

7.2 Non-Solder Mask (Copper) Defined Pad

The non-solder mask (or copper) defined pad has a solder mask opening larger than the copper area. With this method, the pad periphery is left under the control of the etching process. As expected, this method is generally not as accurate as the solder mask photo image control described above. Although pad size varies more than with the SMD method, the pads can be made smaller for the same ball area. This allows additional line routing space between pads. Pattern registration is also more accurate with this method. This may be an advantage to vision systems since registration on copper reference points will give the exact location of the site. Relying on the solder mask can cause miscues because of variances in the site location relative to vision reference points.

7.3 196-pin BGA Routing and Pad Size

The 196-pin BGA package is more dense than normal BGA packages and provides additional challenges for trace routing. With the 82559 many of these issues are handled by considered die layout. The routing signals are carefully placed in the periphery to minimize routing congestion. Signals are also grouped by function to minimize any need to route digital and analog signals together.

Figure 10 shows the relational groupings. The box outline contains the PCI signal group. These signals can easily be routed to the PCI connector without interfering with the analog routing area. This can be observed in actual practice on a sample network card layout provided in Appendix A. One of the primarily design goals in developing the 82559 was to reduce the cost of 10/100 Mbps Ethernet connections. Therefore, power, die, and real estate requirements were achieved without severely impacting layout complexity.

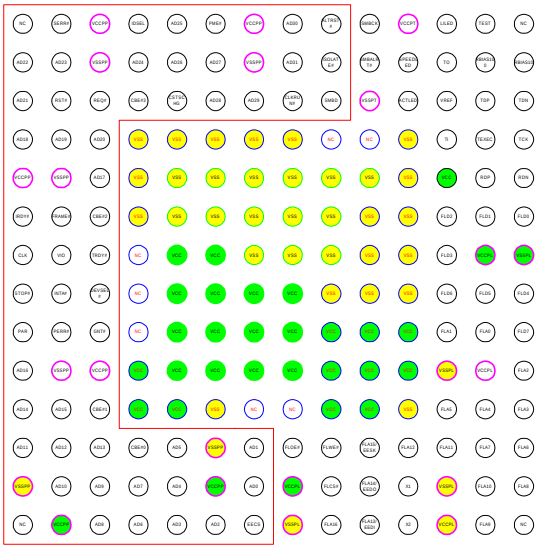


Figure 10. 82559 Ball Pattern

Table 1 summarizes general design rules for design provided in Appendix A.

Table 1. 82559 General Design Rules

Pad Information	Drill	Pads	Anti-pads
BGA pads	Not applicable	0.018 inch	Not applicable
BGA vias	0.010 inch	0.020 inch	0.032 inch
Standard vias	0.010 inch	0.032 inch	0.044 inch

NOTE: 82559 Micro BGA Pattern:
Number of balls (pins) = 196
Ball pitch = 1 mm (0.0394 inch)
Traces = 0.006 inch
Trace spacing = 0.006 inch

7.3.1 Top Layer Routing

Figure 11 shows the top side routing paths for the signals in the reference layout. (The complete layout is contained in Appendix A.) In this diagram 6 mil traces are used to bring the signals from the 18 mil ball pads out to 20 mil via pads. The vias use a 10 mil drill though the 20 mil pad.

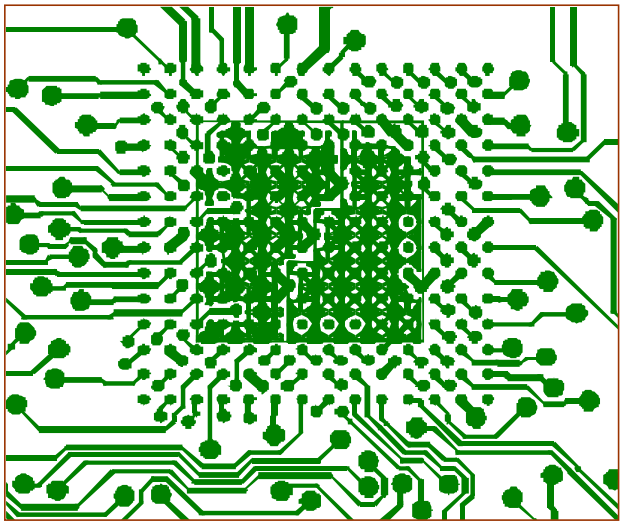


Figure 11. 82559 Top Layer Routing

Note: Sensitive analog signals are routed completely on the top layer without the use of vias. This allows tight control of signal integrity and removes any impedance inconsistencies due to layer changes.

Note: The power plane connections use the top side planes to minimize the number of vias required. One via per power connection would be optimal; however, this is almost impossible to achieve due to the tight grid internal to the device.

7.3.2 Bottom Layer Routing

Figure 12 shows the bottom side routing paths from the vias. As mentioned previously, an attempt to limit these signals was made. These signals have a higher tolerance for impedance incongruences.

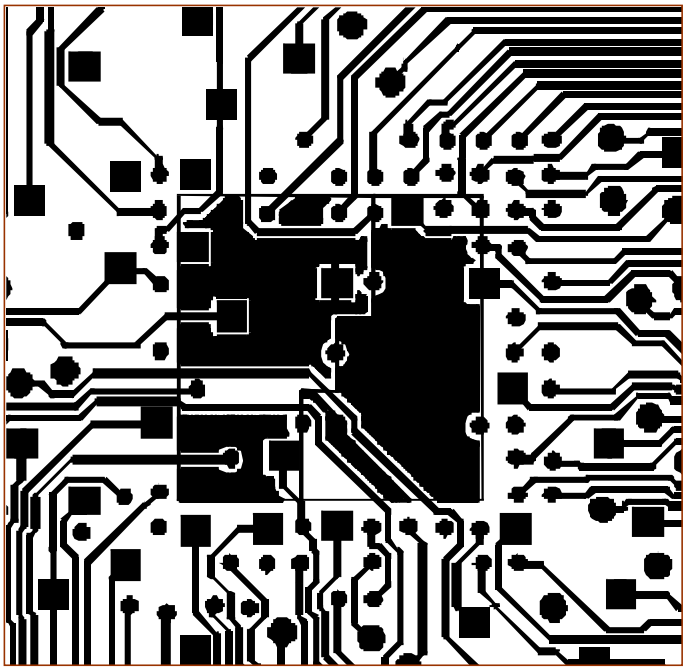


Figure 12. 82559 Bottom Layer Routing

7.3.3 Analog Signal Routing

The analog signals from the 82559 to the magnetics module are the most critical routing path. The second most critical path from the magnetics module to the RJ-45. Controlling signal path anomalies such as impedance, cross-talk, and EMI will increase performance. Analog signals from the 82559's PHY unit should run to the line interface components, not through any vias. In addition to this restriction, these signals should be routed avoiding possible interference from neighboring signals.

Generally, differential pairs (for example, TDP/TDN and RDP/RDN) should be routed prior to starting any other layout. This ensures that a reasonable keep-out zone for other signals can be maintained. Figure 13 shows the route of these signals in the reference layout.

Trace spacing, trace length, as well as avoidance of digital signals was maintained. In this example, a single small surface mount termination resistor is placed directly across the signal pairs to help avoid reflections from trace bends or stubs.

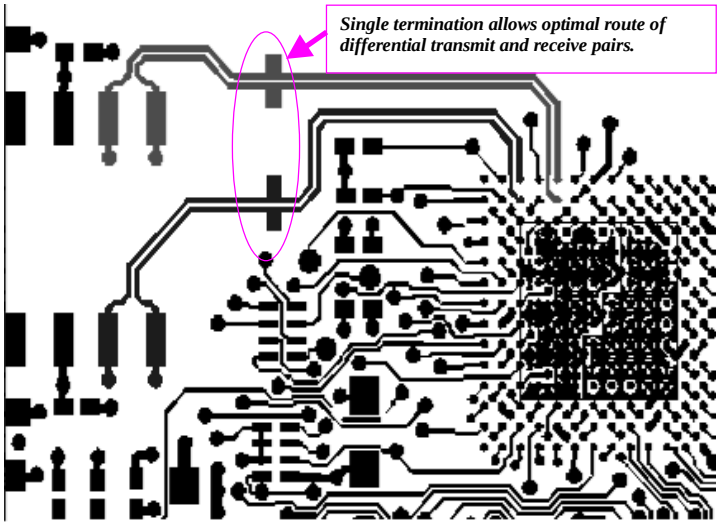
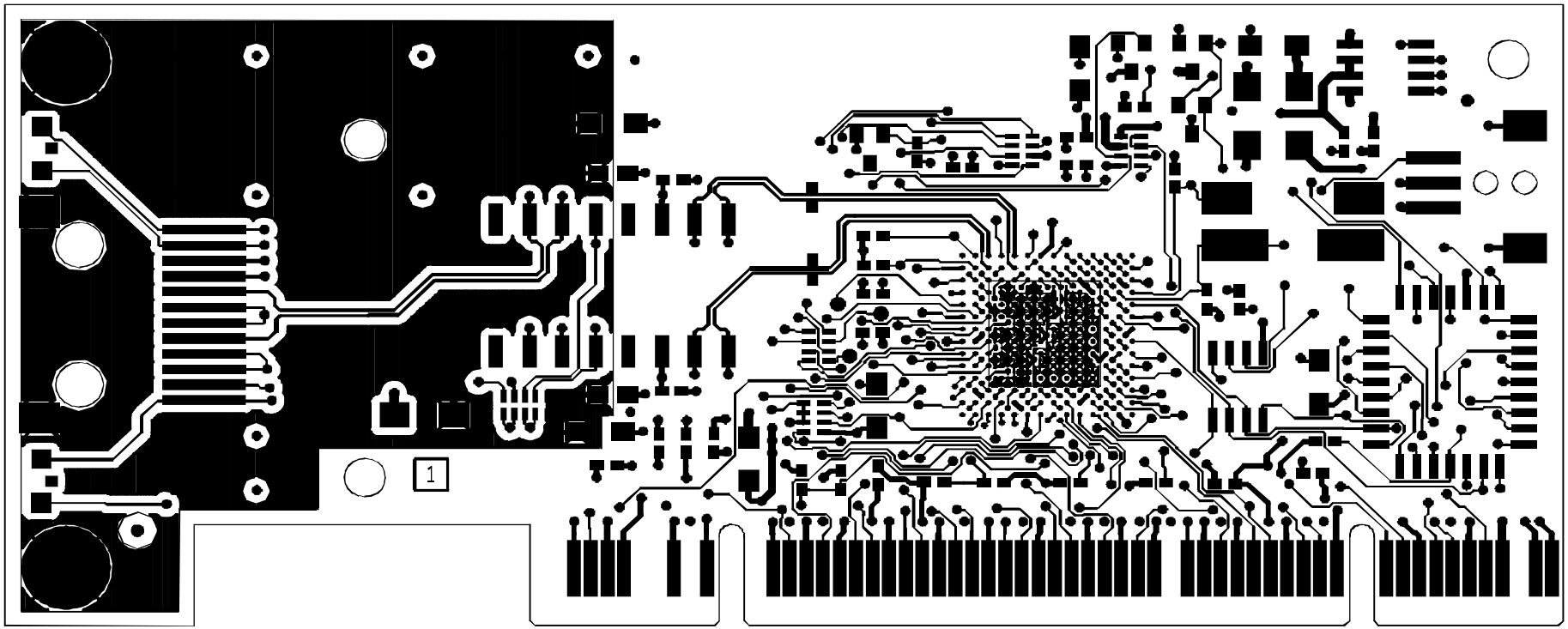


Figure 13. 82559 Analog Signal Routing

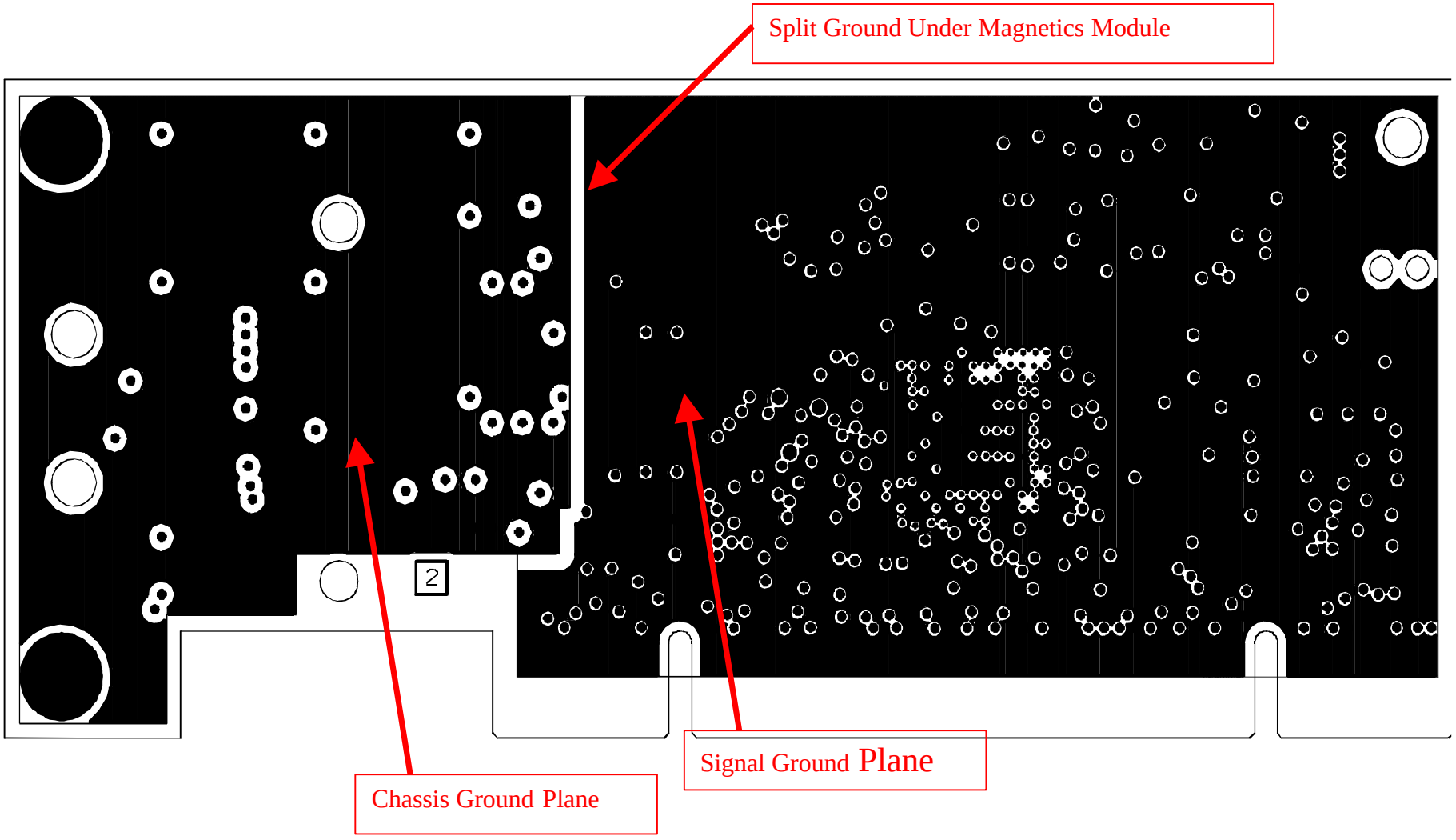
Appendix A 82559 Layout Diagrams

This appendix contains the following diagrams:

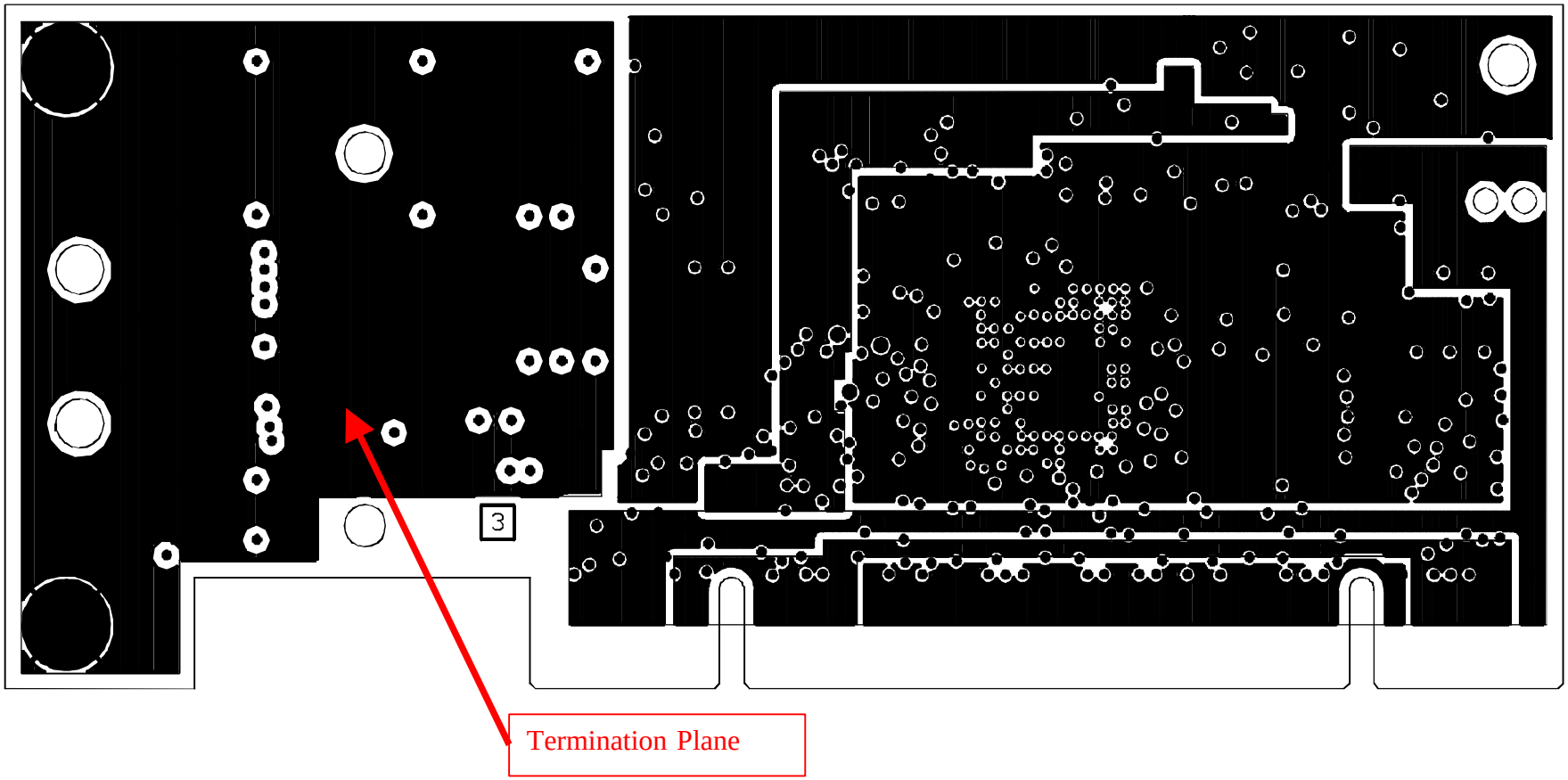
- Sample Network Card Layer 1 (Top Side Layout)
- Sample Network Card Layer 2 (Ground Plane Layout)
- Sample Network Card Layer 3 (Power Plane Layout)
- Sample Network Card Layer 4 (Backside Layout)
- Sample Network Card Fabrication



Sample Network Card Layout Top Side View

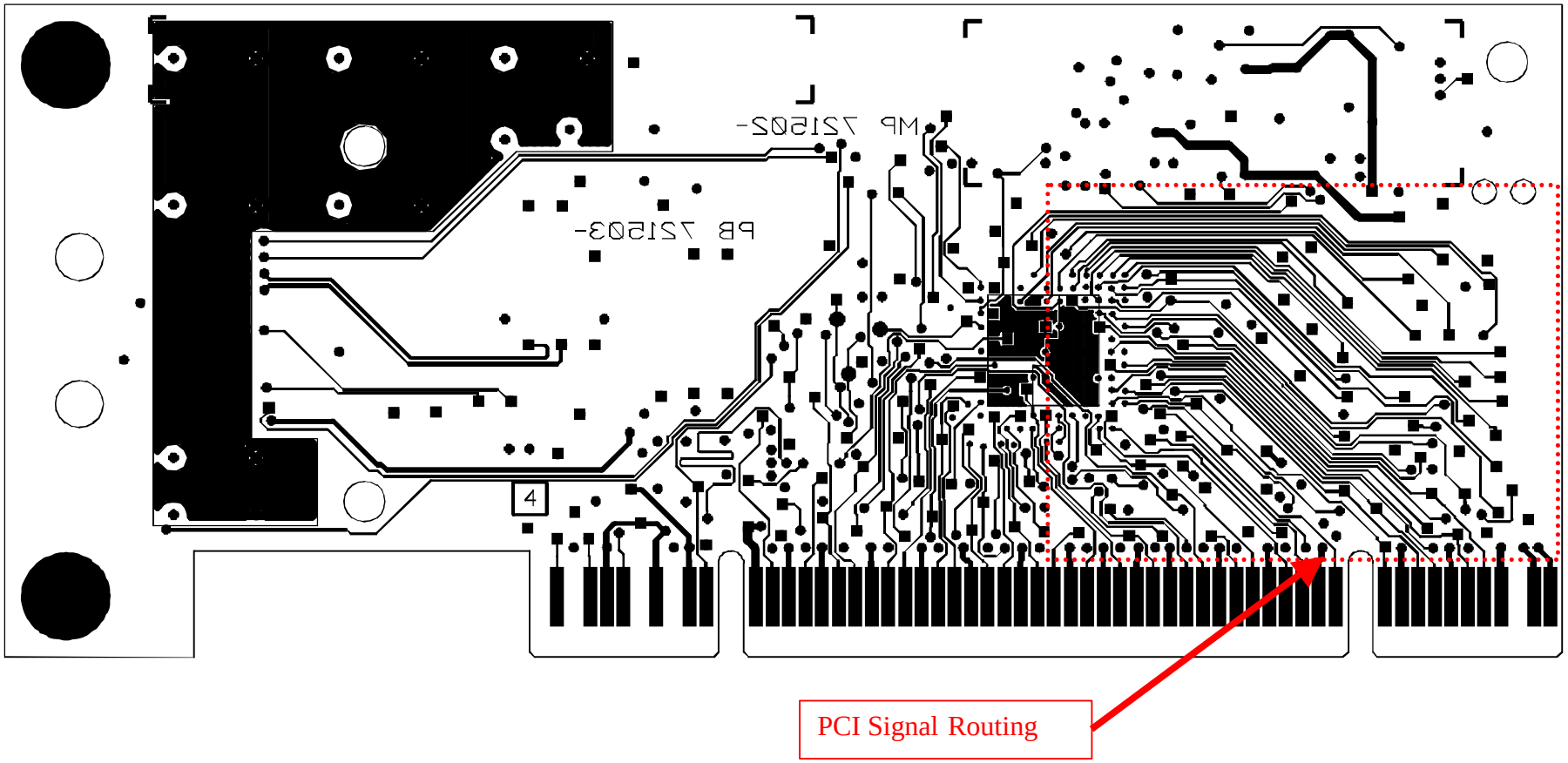


Sample Network Card Layout Layer 2 (Ground Plane)

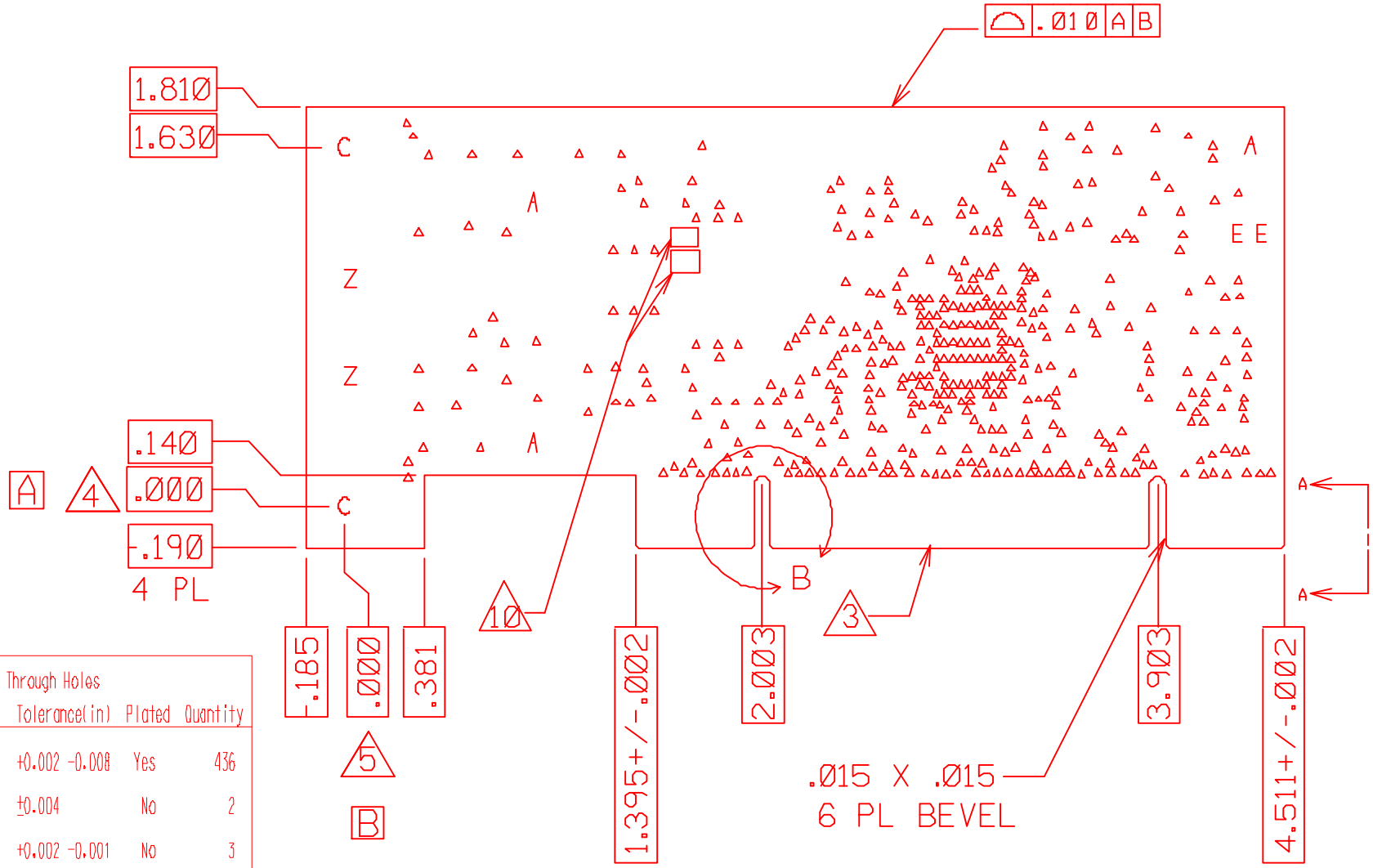


Sample Network Card Layout Layer 3 (Power Plane)

Note: This layout uses a split power plane to route one of three voltage sources to a voltage regulator. The 82559 is sourced from the output of the voltage regulator.



Sample Network Card Layout Layer 4 (Backside)



Through Holes

Symbol	Diameter(in)	Tolerance(in)	Plated	Quantity
Δ	0.0100	+0.002 -0.008	Yes	436
Z	0.1460	±0.004	No	2
A	0.1250	+0.002 -0.001	No	3
C	0.1250	±0.002	Yes	2
E	0.0750	±0.004	No	2

Sample Network Card Fabrication Drawing