# PL-2519
# Hi-Speed USB Video Cam and Flash Disk Controller IC

## Product Datasheet

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# Revision History

| Revision | Description | Date |
|---|---|---|
| 1.2 | ➢ [Section 3.3 SRAM Interface Timing] – Change maximum value of “output enable to data in valid” from 8.5 to 10. | November, 2003 |
| 1.1 | ➢ Change Package Outline to CF BGA 256pin | November, 2003 |
| 1.0 | ➢ Initial Draft | October, 2003 |

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# 1.0 Features

- MPEG-4 Video Recorder at CIF (352x288) resolution up to 30 frames per second
- 128MB memory can store up to 42 minutes of Video at 384kbps and ADPCM Audio
- User-Configurable Compression Bit Rate
- Supports AVI file format playback thru Windows Media Player
- ADPCM Voice Recording and Playback
- Supports NAND Flash or xD-Picture Card
- Supports external EEPROM for Vendor/Product related information customization
- On-chip USB2.0 Device Controller
- Advanced 8032 Microcontroller
- Mass Storage Class compatible: no manufacturer driver needed for Linux, Mac OS 8.6, Windows ME, 2000, XP or above OS versions. Windows 98 requires separate driver.
- 8-bit YCbYCr 4:2:2 CMOS Sensor Interface
- Still Image Capture (snap shot) in JPEG format after uploading to PC
- PC Web Cam for instant Messenger application
- On chip 3.3V-2.5V 150mA Regulator for internal circuit
- Capable of interfacing up to eight state-of-the-art NAND Flash Memories
- Package type: LF BGA 256 pin.

## 1.1 Block Diagram

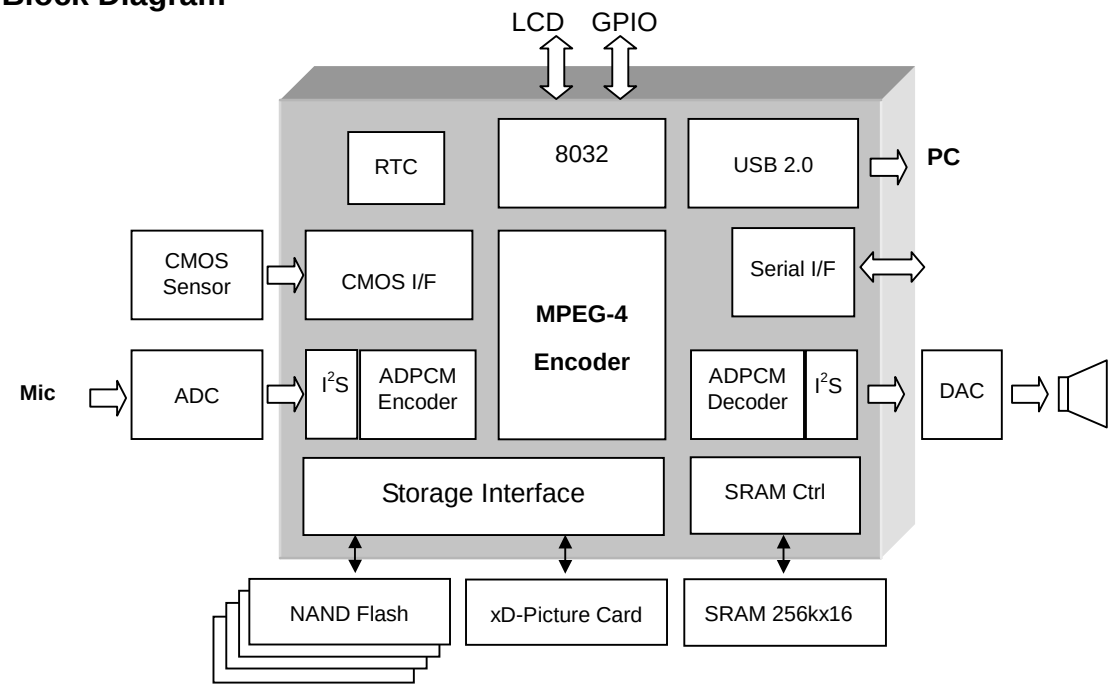



**Figure 1-1 Block Diagram of PL-2519**

## 2.0 Overview

The PL-2519 controller is a highly integrated Hi-Speed USB chip specially designed for portable digital multimedia devices such as MPEG-4 video cameras, digital voice recorders and flash memory drives. The PL-2519 controller is compliant with MPEG-4 Simple Profile (Level 1 to Level 3) and supports CIF (352x288) resolution up to 30 frames per second. High compression rate allows 128MB flash memory to store up to 42 minutes of high quality video and audio. Users can also use the snap shot function to capture still images and ADPCM encoding to record voice data, and save them directly to the flash memory or xD-Picture card. The PL-2519 is compliant with USB mass storage class drivers so users can instantly plug-in the device to the PC and easily exchange data, graphics, texts or digital images stored in the NAND Flash or xD-Picture cards.


**Figure 2-1 Sample Application of PL-2519**

## 2.1 Function Specifications

| Function | Specification |
|---|---|
| USB Interface | USB 2.0, On chip USB2.0 PHY |
| Regulator | On chip 3.3V to 2.5V 150mA regulator for internal circuit. |
| NAND Flash Interface | Supports up to eight state-of-the-art NAND Flash memories. |
| USB Device Class | Mass Storage Class compatible, no driver needed for MAC OS 8.6, Windows ME, 2000, XP or above OS versions. Windows 98 have to install separate driver. |
| CMOS Sensor interface | 8-bit 4:2:2 YCbYCr mode (similar to CCIR601).<br>The input frame rate should keep at 30fps and the maximum pixel clock rate is 24MHz.<br>Currently uses IC Media ICM202B or Omni-Vision OV7648 CMOS sensor. |
| Video Encoder | MPEG-4 Simple Profile (L1~L3) compliant |
| Audio Codec | IMA ADPCM compatible |
| Video Resolution | Supports following resolutions at 30 frames/sec:<br>• CIF 352x288<br>• QCIF 176x144<br>• QVGA 320x240<br>• QQVGA 160x120<br>Compression bit rate can be configured by user. |
| Captured Still Image Resolution | CIF 352x288 |
| EEPROM | Store program for functional operation.<br>(Max. 128Kbytes) |
| SRAM | External SRAM 256Kx16bits |
| File System | FAT16 |
| GPIO | Supports GPIO for User Interface (UI) buttons and LCD display menu operations. |
| RTC (+Timer) | For real-time display |
| Power Management | Advanced power management mechanism |
| PC Minimum Requirement | Pentium II 350MHz |
| PC OS Minimum Requirement for Video Playback | Microsoft recommends that users who are running Microsoft Windows 98, Microsoft Windows Millennium Edition (Me), or Microsoft Windows 2000 download the Windows Media Player 7.1 to properly playback contents that were created with the latest Windows Media audio and video codecs. |

# 3.0 Pin Assignment and Description

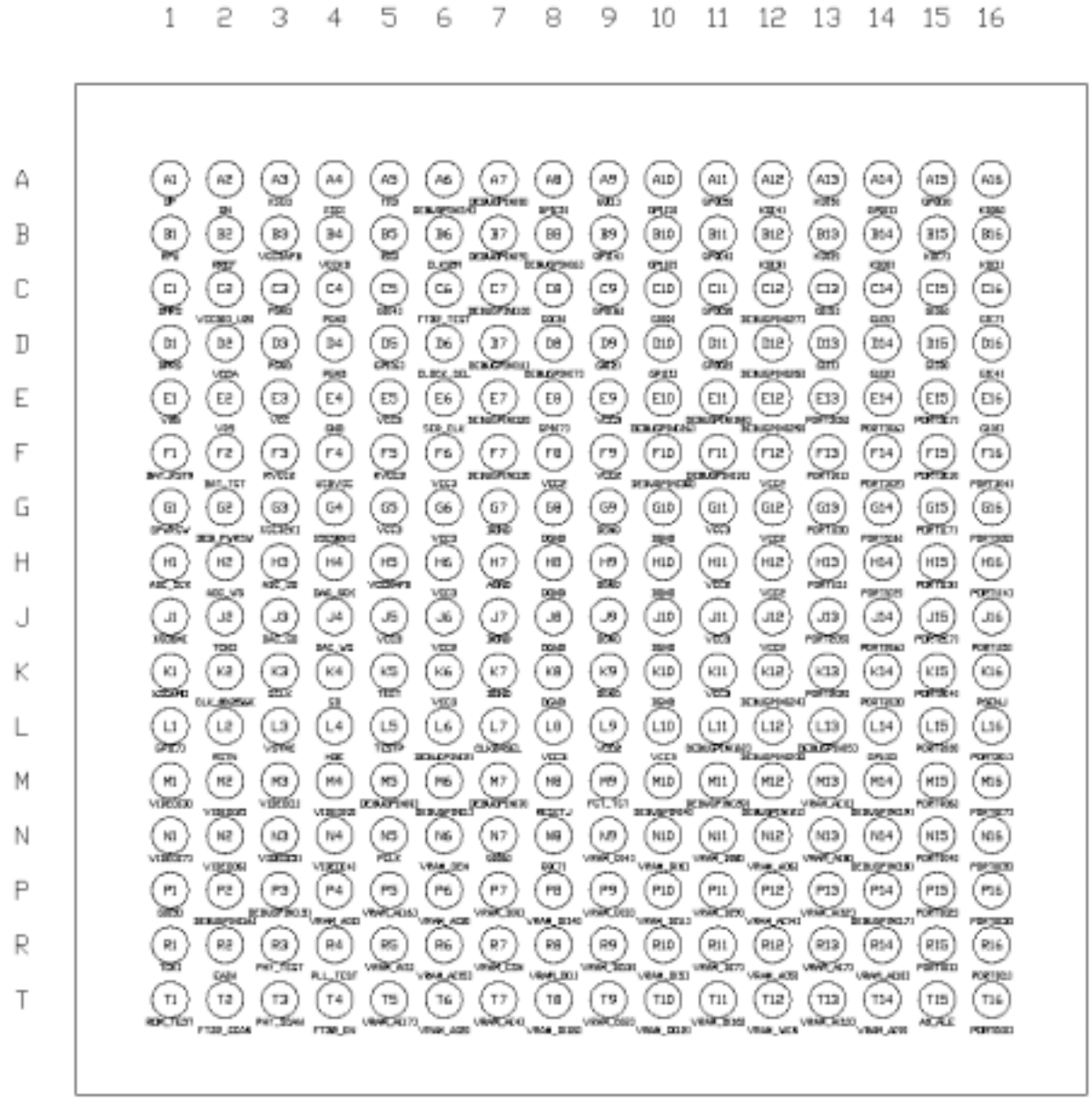



**Figure 3-1 Pin out diagram of PL-2519**

**Table 3-1 Pin description of PL-2519**

| Pin | Symbol | Type | Description |
|---|---|---|---|
| **PHY 2.0 Interface:** | | | |
| B6 | CLK12M | O | 12MHz clock output to PHY. Connected to XSCI (pin A4). |
| A4 | XSCI | I | Crystal input. Connected to CLK12M (pin B6) .The input frequency is 12MHz. |
| A3 | XSCO | O | Crystal output. NC. |
| B4 | VCCKB | P | Digital power pin. Connected to 2.5V power. |
| C3, C4, D3, D4 | PGND | P | PHY ground pin. Connected to ground. |
| B3 | VCC3APB | P | Analog power pin. Connect to 3.3V power. |
| B2 | RREF | I | Connect external reference resister (12.1Kohm ± 1%) to Analog GND. |
| A2 | DN | I/O | USB2.0 Data negative pin. |
| A1 | DP | I/O | USB2.0 Data positive pin. |
| B1 | RPU | I | Connect external resister (1.5Kohm ± 0.1%) to B3 (Analog 3.3V power). |
| C1 | DMRS | I/O | USB2.0 Data negative pin, connect to external resister (39ohm ± 0.1%). |
| D1 | DPRS | I/O | USB2.0 Data positive pin, connect to external resister (39ohm ± 0.1%). |
| C2 | VCC3IO_U20 | P | Analog power pin. Connected to 3.3V power. |
| D2 | VCCA | P | Analog power pin. Connected to 3.3V power. |
| **3.3V to 2.5V Regulator:** | | | |
| E4 | GND | P | Regulator ground |
| E3 | VCC | P | 3.3V power input |
| E1,E2 | V25 | P | 2.5V power output. (E1 and E2 are tied together internally.) |
| **Real Time Clock (RTC) Interface – Individual Power Plane:** | | | |
| F5 | RVCC3 | P | 3.3V power input. |
| F4 | USBVCC | I | Connect to USB power, it is use to detect the USB bus power. And should be short to GP0[7]. |
| F3 | RVCC2 | P | RTC digital 2.5V power input. |
| F2 | BAT_TST | I | RTC function test. Connect to ground. |
| F1 | BAT_RSTN | I | RTC reset, low active. |
| G1 | GPWRSW | I | Power on switch button. |
| G2 | DEB_PWRSW | O | De-bounced power switch. Use to turn on system power. |
| G3 | XSC32KI | I | 32KHz crystal input. |
| G4 | XSC32KO | O | Crystal output. |

***continue next page…***

**Table 3-1 Pin description of PL-2519 (cont…)**

| Pin | Symbol | Type | Description |
|---|---|---|---|
| **CMOS Sensor Interface:** | | | |
| L2 | RSTN | O | Output to CMOS sensor system reset, low active. |
| J2 | TCKO | O | Output to CMOS sensor clock. |
| N5 | PCLK | I | Pixel clock input. |
| L3 | VSYNC | I | Vertical sync input. |
| L4 | HDE | I | Horizontal display Enable input. |
| N1, N2, N3, N4, M1, M2, M3, M4 | VIDEO[7:0] MSB:LSB | I | Video Data Input. |
| **Video RAM (SRAM) Interface:** | | | |
| R7 | VRAM_CSN | O | Video RAM chip select, low active. |
| N6 | VRAM_OEN | O | Video RAM output enable, low active. |
| T5, P5, R6, P12, T13, P13, M13, R14, T14, N13, R13, N12, R12, T7, P6, T6, R5, P4 | VRAM_A[17:0] MSB:LSB | O | Video RAM Address. |
| T8,P8,R9, T10,P10, T11,P11, N11,R11, N10,R10, N9,P9,T9, R8,P7 | VRAM_D[15:0] MSB:LSB | I/O | Video RAM Data. |
| T12 | VRAM_WEN | O | Video RAM write enable, low active. |

***continue next page…***

**Table 3-1 Pin description of PL-2519 (cont…)**

| Pin | Symbol | Type | Description |
|---|---|---|---|
| **8032 Micro-Controller Interface:** | | | |
| D6 | CLOCK_SEL | I | Select the operating clock of 8032.<br>1: The 8032 operates in 48MHz<br>0: The 8032 operates in 24MHz<br>Normally, tied to ground. |
| R2 | EAIN | I | External access, connect to 3.3V power. |
| T4 | FT32_EN | I | Internal 8032 enable, connect to 3.3V power. |
| T15 | A0_ALE | O | Address latch enable |
| M16, M15, N16, N15, P16, P15, (R15, R16) T16 | PORT0[7:0] MSB:LSB | I/O | port0. (address[7:0]/data bus[7:0])<br>R15 and R16 are tied together internally. |
| G15, G14, G13, H16, H15, H14, H13, J16 | PORT1[7:0] MSB:LSB | I/O | port1[7:0] |
| J15, J14, J13, K15, K14, K13, L16, L15 | PORT2[7:0] MSB:LSB | I/O | port2[7:0]. (address[15:8]) |
| E15, E14, E13, F16, F15, F14, F13, G16 | PORT3[7:0] MSB:LSB | I/O | port3[7:0] |
| K16 | PSENJ | O | Program strobe enable |

***continue next page…***

**Table 3-1 Pin description of PL-2519 (cont…)**

| Pin | Symbol | Type | Description |
|---|---|---|---|
| **Nand Flash/XD and GPIO Interface:** | | | |
| B15, A16, A13, A12, B12, B13, B16, B14 | KD[7:0] | I/O | NAND flash data bus[7:0] |
| A15 | GP0[0] | I/O | GPIO pin. Currently, used as NAND flash Read control |
| A14 | GP0[1] | I/O | GPIO pin. Currently, used as NAND flash write enable control |
| D11 | GP0[2] | I/O | GPIO pin. Currently, used as NAND flash command latch enable control |
| C11 | GP0[3] | I/O | GPIO pin. Currently, used as NAND flash address latch enable control |
| B11 | GP0[4] | I/O | GPIO pin. Currently, used as NAND flash R/B (ready/busy) control |
| C9, A11 | GP0[6:5] | I/O | GPIO pin. |
| E8 | GP0[7] | I/O | GPIO pin. Currently, it is use to detect USB connection. |
| L14 | GP1[0] | I/O | GPIO pin. Currently, used as NAND flash write protect in. |
| B10, D10 | GP1[2:1] | I/O | GPIO pin. |
| A10 | GP1[3] | I/O | GPIO pin. Currently, used as NAND flash security input. |
| L1, D5, A8, B9 | GP1[7:4] | I/O | GPIO pin. |
| N8, N7, P1, C5, C8, D9, A9, C10 | G0[7:0] | I/O | GPIO pin. Currently, used as LCD display control pin. |
| D15, D14, D13, E16 | G1[3:0] | I/O | GPIO pin. Currently, used as LCD display control pin. |
| D16 | G1[4] | I/O | GPIO pin. Currently, used as NAND flash chip select 0. |
| C13, C14 | G1[5] | I/O | GPIO pin. Currently, used as NAND flash chip select 1. |
| C15 | G1[6] | I/O | GPIO pin. Currently, used as NAND flash operation LED indicator. |
| C16 | G1[7] | I/O | GPIO pin. |
| **RS232 Interface:** | | | |
| A5 | TXD | O | Transmitted data |
| B5 | RXD | I | Received data |

***continue next page…***

**Table 3-1 Pin description of PL-2519 (cont…)**

| Pin | Symbol | Type | Description |
|---|---|---|---|
| **Voice Recorder/Playback Interface:** | | | |
| K2 | CLK_8X256K | O | 256-times sampling clock output for ADC/DAC. |
| H1 | ADC_SCK | O | ADC clock |
| H2 | ADC_WS | O | ADC word select |
| H3 | ADC_SD | I | ADC serial data |
| H4 | DAC_SCK | O | DAC clock |
| J4 | DAC_WS | O | DAC word select |
| J3 | DAC_SD | O | DAC serial data |
| **CPLD Interface:** | | | |
| K3 | SCLK | O | Clock output to CPLD |
| K4 | SD | I/O | Data bus for CPLD |
| **Power/GND Pins:** | | | |
| E5, E9, F6, G5, G6, G11, H6, J5, J11, K6, K11, L8, L10 | VCC3 | P | 3.3V digital power. |
| F8, F9, F12, G12, H11, H12, J6, J12, L9 | VCC2 | P | 2.5V digital power. |
| H5 | VCC2APB | P | 2.5V analog power. (PLL) |
| H7 | AGND | P | Analog ground. |
| G7, G8, G9, G10, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10 | DGND | P | Digital ground. |
| **System Reset and Clock Input:** | | | |
| M8 | RESETJ | I | System reset, low active.<br>PL2519 had build-in a power-on reset circuit. Thus, this pin can be tied to 3.3V digital power. |
| J1 | XSC6MI | I | Crystal input. The input frequency is 6MHz. |
| K1 | XSC6MO | O | Crystal output. |

***continue next page…***

**Table 3-1 Pin description of PL-2519 (cont…)**

| Pin | Symbol | Type | Description |
|---|---|---|---|
| **Test Pins:** | | | |
| T2 | FT32_SCAN | I | 8032 test mode - pull down internally. NC or tied to ground for normal operation. |
| C6 | FT32_TEST | I | 8032 test mode - pull down internally. NC or tied to ground for normal operation. |
| R1 | TCKI | I | PLL test clock input, pull down internally. NC or tied to ground for normal operation. |
| T1 | ROM_TEST | I | Test mode - pull down internally. NC or tied to ground for normal operation. |
| T3 | PHY_SCAN | I | Test mode - pull down internally. NC or tied to ground for normal operation |
| R3 | PHY_TEST | I | Test mode - pull down internally. NC or tied to ground for normal operation |
| R4 | PLL_TEST | I | Test mode - pull down internally. NC or tied to ground for normal operation |
| K5 | TEST | I | Test mode - pull down internally, NC or tied to ground for normal operation |
| L5 | TESTP | I | Test mode - pull down internally. NC or tied to ground for normal operation |
| L7 | CLK24SEL | I | Pull down internally. NC or tied to ground for normal operation |
| M9 | FCT_TST | I | Function test mode - pull down internally. NC or tied to ground for normal operation |
| **Debug Pins:** | | | |
| F11, F10, E12, E11, C12, E10, D12, K12, L12, L11, M12, M11, M14, N14, P14, P2, P3, A6, F7, E7, D7, C7, B7, A7, D8, B8, L13, M10, M7, L6, M6, M5 | DEBUGPIN[31:0] | O | Debug pin. NC |
| E6 | SER_CLK | I/O | Serial clock. NC |

***- End of Table -***

## 3.1 Real Time Clock (RTC)

The RTC circuit is always on and running at 32.768KHz frequency. It contains a 32-bit counter that increases once in every second. The timer can be read or written by the internal 8032 microcontroller. Based on the timer, some time process such as time display can be done by the 8032.

Controlling system power is another function provided by the RTC. When user press the power switch (GPWRSW), the RTC will de-bounce the power switch and turn on the system by the DEB_PWRSW pin. When pressing the power switch again, the system will power off but the RTC will still be running.

## 3.2 CMOS Sensor Interface

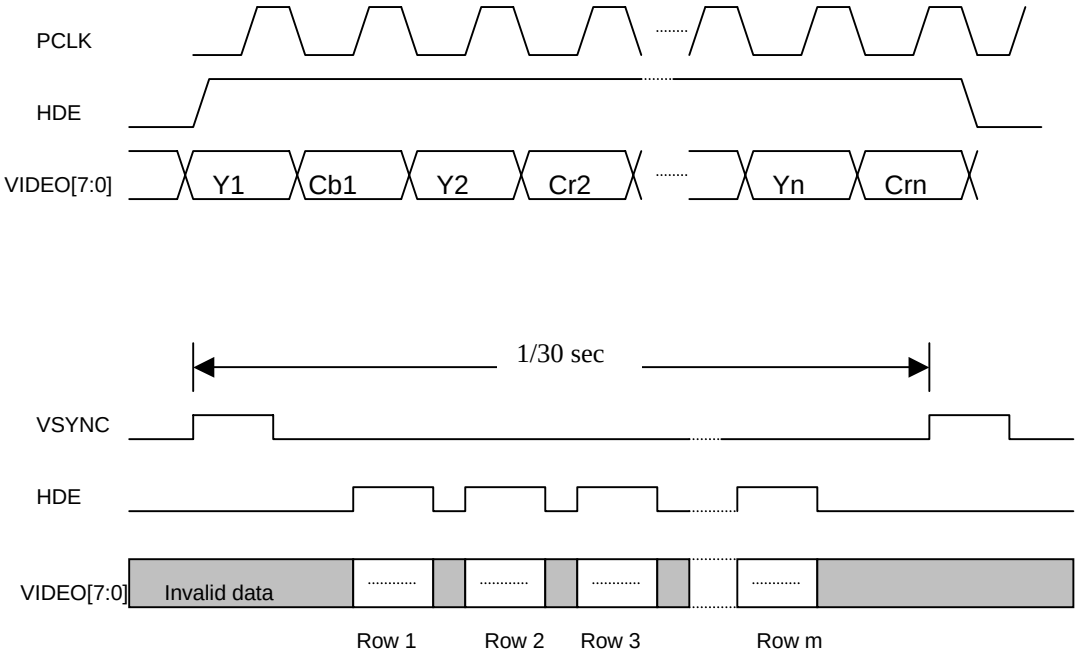



**Figure 3-2 CMOS sensor interface of PL-2519**

The input video data of PL2519 is an 8-bit YCbYCr 4:2:2 mode as shown in Figure 3-2. The Maximum pixel clock (PCLK) is 24MHz and the input sequence is YCbYCr. The HDE (horizontal display enable or horizontal valid data indicator) must be kept high from first valid data to the last one:

- CIF mode: HDE keep high for 704 clock period (n=352), and 288 rows (m=288) per frame.
- QCIF mode: HDE keep high for 352 clock period (n=176), and 144 rows (m=144) per frame.
- QVGA mode: HDE keep high for 640 clock period (n=320), and 240 rows (m=240) per frame.
- QQVGA mode: HDE keep high for 320 clock period (n=160), and 120 rows (m=120) per frame.

As for the VSYNC requirement, it must be kept at 30 frames/sec because it is used as the time base for MPEG4 bit rate control.

## 3.3 SRAM Interface Timing

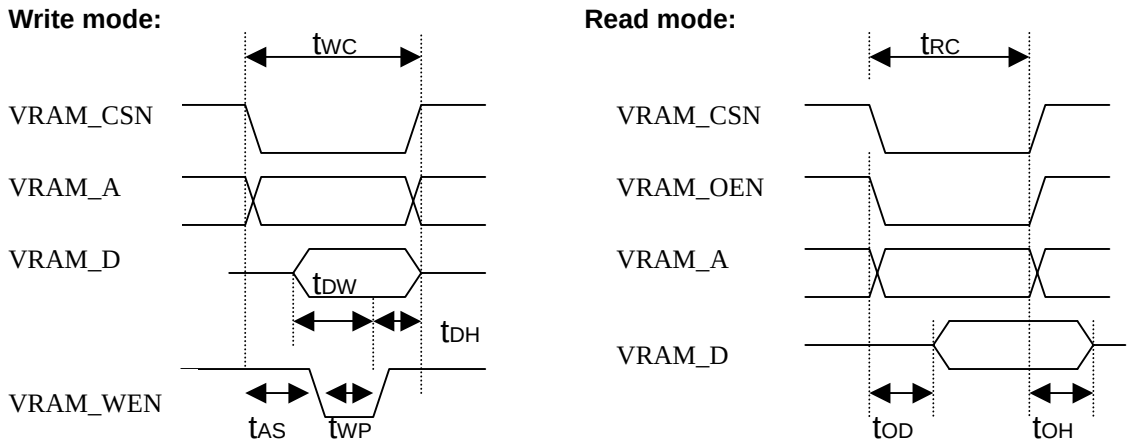


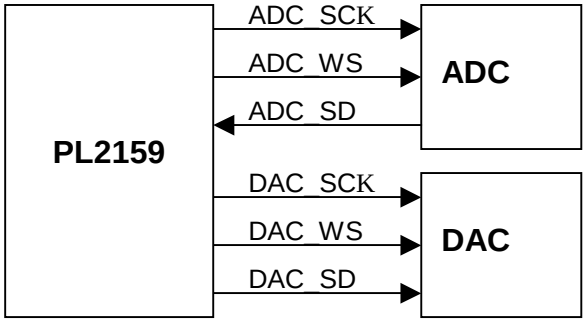

**Figure 3-3 SRAM Interface Timing of PL-2519**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Write cycle time | $t_{WC}$ | 20 | - | ns |
| Data to write time overlay | $t_{DW}$ | 10 | - | ns |
| Data hold from write | $t_{DH}$ | 6 | - | ns |
| Address setup time | $t_{AS}$ | 1 | - | ns |
| Write pulse width | $t_{WP}$ | 8 | - | ns |
| Read cycle time | $t_{RC}$ | 20 | - | ns |
| Output enable to data in valid | $t_{OD}$ | - | 10 | ns |
| Output hold output enable change | $t_{OH}$ | 0 | - | ns |

## 3.4 Voice Recorder/Playback Interface

PL2519 accepts several industry standard audio data formats with 8 to 20-bit data, MSB/LSB-justified, I2S, etc., providing easy interface for audio ADC/DAC/CODEC devices. Sampling rates up to 50KHz are supported.

**Application 1:**




**Application 2:**

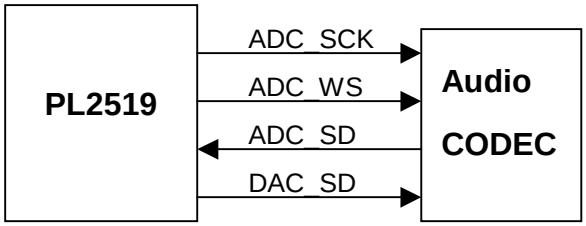



**Figure 3-4 Voice/Recorder Playback Interface of PL-2519**

## 3.5 CPLD interface

The CPLD interface is used to extend the GPIO pins or functions of the PL-2519. Through the use of 2 pins – SCLK (serial clock) and SD(serial data), protocol defined by Prolific, the 8032 microcontroller can read/write registers or control the CPLD logic easily. For more information, contact Prolific Technology Inc.

# 4.0 DC Characteristics

## 4.1 Absolute Maximum Ratings

**Table 4.1 Absolute Maximum Ratings**

| SYMBOL | PARAMETER | RATING | UNITS |
|---|---|---|---|
| VCC | Power Supply | -0.3 to VCC+0.3 | V |
| AVcc3 | Power Supply | -0.3 to 3.6 | V |
| Vin | Input Voltage of 3.3V I/O with 5V Tolerance | -0.3 to 5.5 | V |
| Vout | Output Voltage | -0.3 to Vcc+0.3 | V |
| Tstg | Storage Temperature | -40 to 150 | C |

## 4.2 Recommended Operation Conditions

**Table 4.2 Recommended Operatrion Conditions**

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| VCCK | Core Power Supply | 2.25 | 2.5 | 2.75 | V |
| VCC2I | Power Supply of 2.5V I/O | 2.25 | 2.5 | 2.75 | V |
| VCC2O | Power Supply of 2.5V I/O | 2.25 | 2.5 | 2.75 | V |
| VCC3I | Power Supply of 3.3V I/O | 3.0 | 3.3 | 3.6 | V |
| VCC3O | Power Supply of 3.3V I/O | 3.0 | 3.3 | 3.6 | V |
| Vin | Input Voltage of 3.3V I/O with 5V Tolerance | 0 | 3.3 | 5.25 | V |
| Tj | Commercial Junction Operation Temperature | 0 | 25 | 115 | C |

## 4.3 General DC Characteristics

**Table 4.3 General DC Characteristics**

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Iin | Input leakage current | No pull-up or pull-down | -10 | | 10 | uA |
| Ioz | Tri-state leakage current | | -10 | | 10 | uA |
| Cin | Input capacitance | | | 3.1 | | pF |
| Cout | Output capacitance | | | 3.1 | | pF |
| Cbid | Bi-directional buffer capacitance | | | 3.1 | | pF |

*Note: The capacitance listed above does not include PAD capacitance and package capacitance.*

## 4.4 DC Electrical Characteristics for 3.3V Operation

**Table 4.4 DC Electrical Characteristics for 3.3V Operation**

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Vil | Input low voltage | LVTTL | | | 0.8 | V |
| Vih | Input high voltage | LVTTL | 2.0 | | | V |
| Vt- | Schmitt trigger negative going threshold voltage | LVTTL | 0.8 | 1.10 | | V |
| Vt+ | Schmitt trigger positive going threshold voltage | LVTTL | | 1.6 | 2.0 | V |
| Vol | Output low voltage | $I_{OL}$= 2, 4, 8, 12, 16, 24 mA | | | 0.4 | V |
| Voh | Output high voltage | $I_{OL}$= 2, 4, 8, 12, 16, 24 mA | 2.4 | | | V |
| Ri | Input pull-up/pull-down resistance | $V_{IL}$= 0v or $V_{IH}$= Vcc | 40 | 75 | 190 | KΩ |

# 5.0 Package Dimensions

## 5.1 CF BGA 256-Pin Package Dimension Diagram

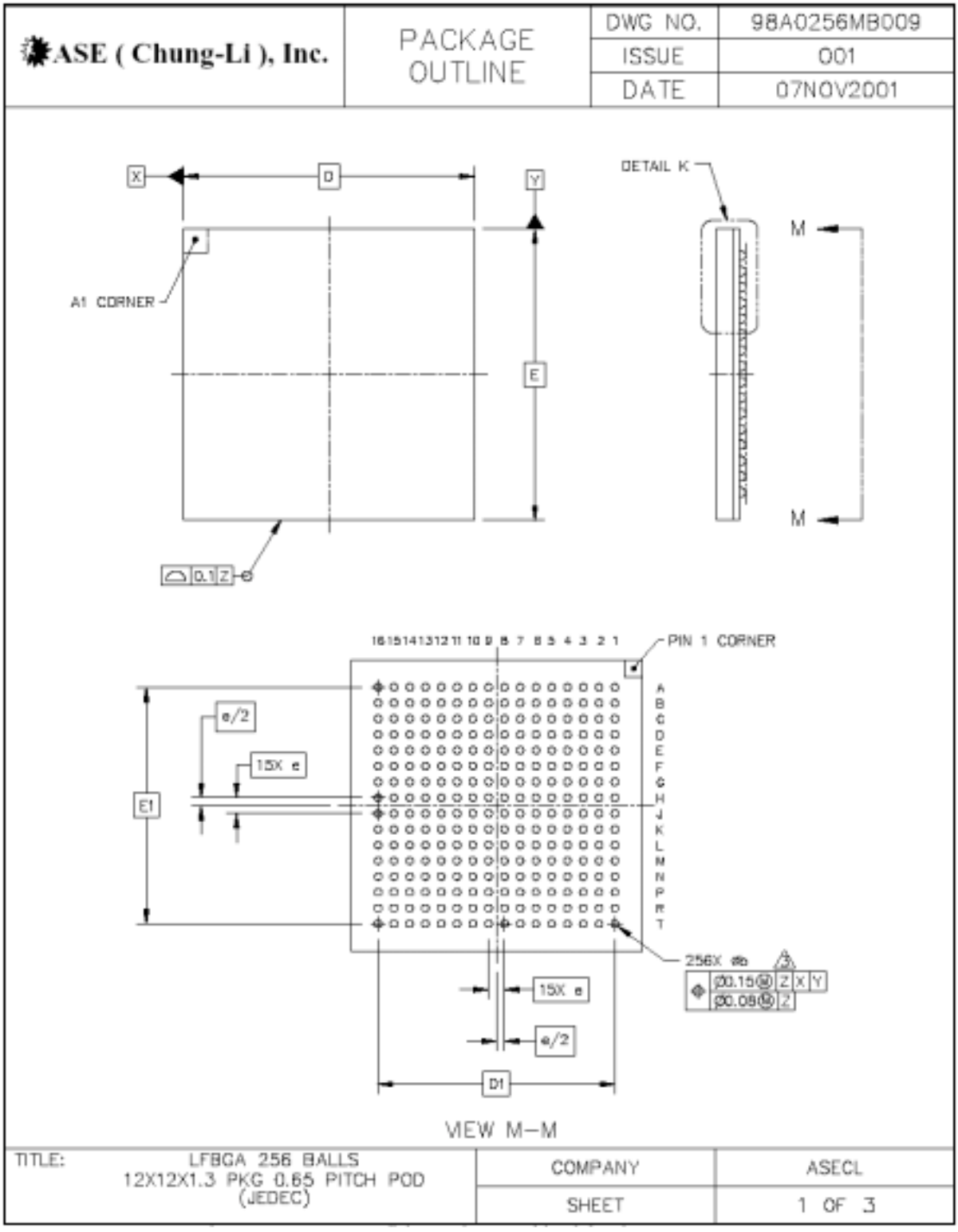
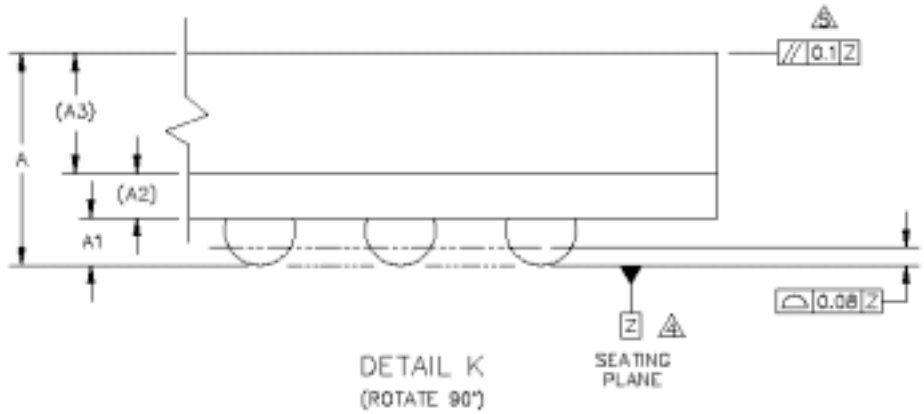



**Figure 5-1a Package Dimension of PL-2519**

| ASE ( Chung-Li ), Inc. | PACKAGE OUTLINE | DWG NO. | 98A0256MB009 |
|---|---|---|---|
| | | ISSUE | 001 |
| | | DATE | 07NOV2001 |




| DIM | MIN | MAX |
|---|---|---|
| A | 0.95 | 1.3 |
| A1 | 0.15 | 0.25 |
| A2 | 0.26 REF | |
| A3 | 0.7 REF | |
| b | 0.25 | 0.35 |
| D | 12 BSC | |
| E | 12 BSC | |
| e | 0.65 BSC | |
| D1 | 9.75 BSC | |
| E1 | 9.75 BSC | |

NOTES

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

| UNIT | DIMENSION AND TOLERANCES | REFERANCE DOCUMENT |
|---|---|---|
| MM | ASME Y14.5M | 98A0232MB002–001 |

| TITLE: LFBGA 256 BALLS 12X12X1.3 PKG 0.65 PITCH POD (JEDEC) | COMPANY | ASECL |
|---|---|---|
| | SHEET | 2 OF 3 |

**Figure 5-1b Package Dimension Diagram of PL-2519**