PL-3507 Combo USB 2.0 / IEEE1394 to IDE Bridge Controller

Product Datasheet

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Revision History

Revision	Description	Date
1.3	➢ Correct UDMA Mode info to UDMA 0-6.	08/2003
1.2	➢ Change to ATA/ATAPI-7 Compliant. ➢ Change pin 14 - GP0[7] (USBVCC) resistor from 10K to 100-ohm.	07/2003
1.1	Correct LQ128 Package Outline Diagram (14 x 14 x 1.4mm)	09/2002
1.0	Customer Release – add DC Characteristics	09/2002
0.9	Preliminary Release – PL3507 Combo USB 2.0 / IEEE1394 to IDE Bridge Controller	09/2002

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1.0 Features

- Provides hot-swap function to select active device USB or 1394.
- Provides auto-detect function to select active device between USB and 1394.
- IEEE 1394-1995 and IEEE P1394a compliant.
- USB 1.1 and USB 2.0 compliant.
- USB Mass Storage Class Bulk-Only Transport Specification Compliant.
- Generic driver support for Microsoft Windows 98SE above, Apple MacOS and Linux. (Windows 98SE need vendor driver for USB)
- AT Attachment with Packet Interface Extension (ATA/ATAPI-7) Compliant
- ATA/ATAPI interface supports PIO mode 0-4, DMA mode 0-2 and Ultra DMA mode 0-6.
- Built-in hardware automated SBP2 protocol engine for 1394 connection which includes:
  - Management ORB fetch engine.
  - Command ORB fetch engine.
  - Page table fetch engine.
  - Response packet generate engine.
- Built-in USB 1.1 & 2.0 PHY.
- 4k bytes of shared data FIFO for USB/1394.
- Embedded 8-bit micro controller.
- Support external serial EEPROM to customize vendor/product related information.
- On-Chip 3.3V to 2.5V regulator.

2.0 Product Overview

The PL-3507 is a high performance combo bridge solution for connecting USB 2.0 and 1394 to ATA or ATAPI data storage devices, e.g. hard disk drives, CD-ROM, CD-R, CD-RW and DVD. The USB interface of PL-3507 supports USB 1.1 or USB 2.0 specifications to allow connections to host computer via USB port at maximum data transfer rate 480 Mbps.

The 1394 interface of the PL-3507 is in compliant with IEEE Std 1394-1995 and IEEE P1394a specification supporting data transfer rate 100, 200 and 400 Mbps, and built-in SBP2 (Serial Bus Protocol 2) hardware engine to enhance sustained data transfer rate up to 40 MByte/sec.

The ATA/ATAPI interface provides signaling and timing for PIO mode 0-4, DMA mode 0-2, and Ultra DMA mode 0-6.

3.0 Functional Block Diagram

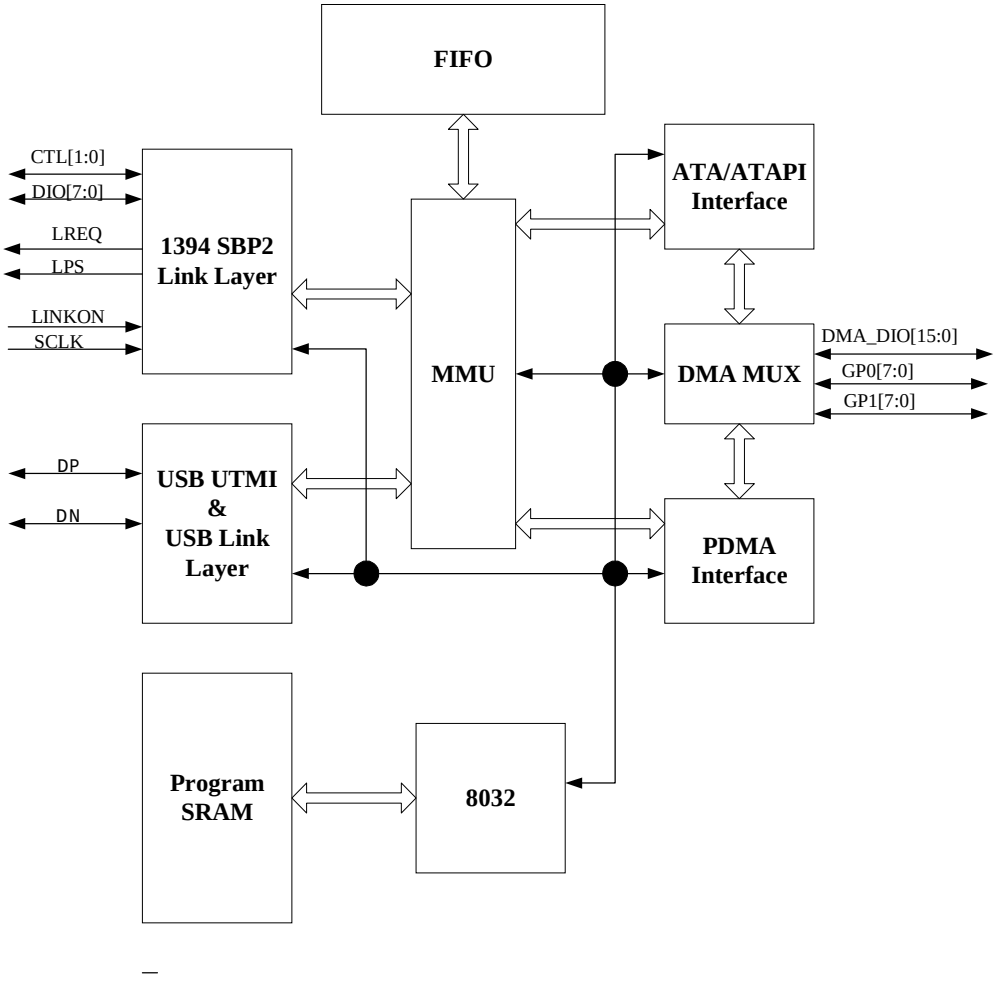


Figure 1-1 Block Diagram of PL-3507

4.0 System Application Diagram

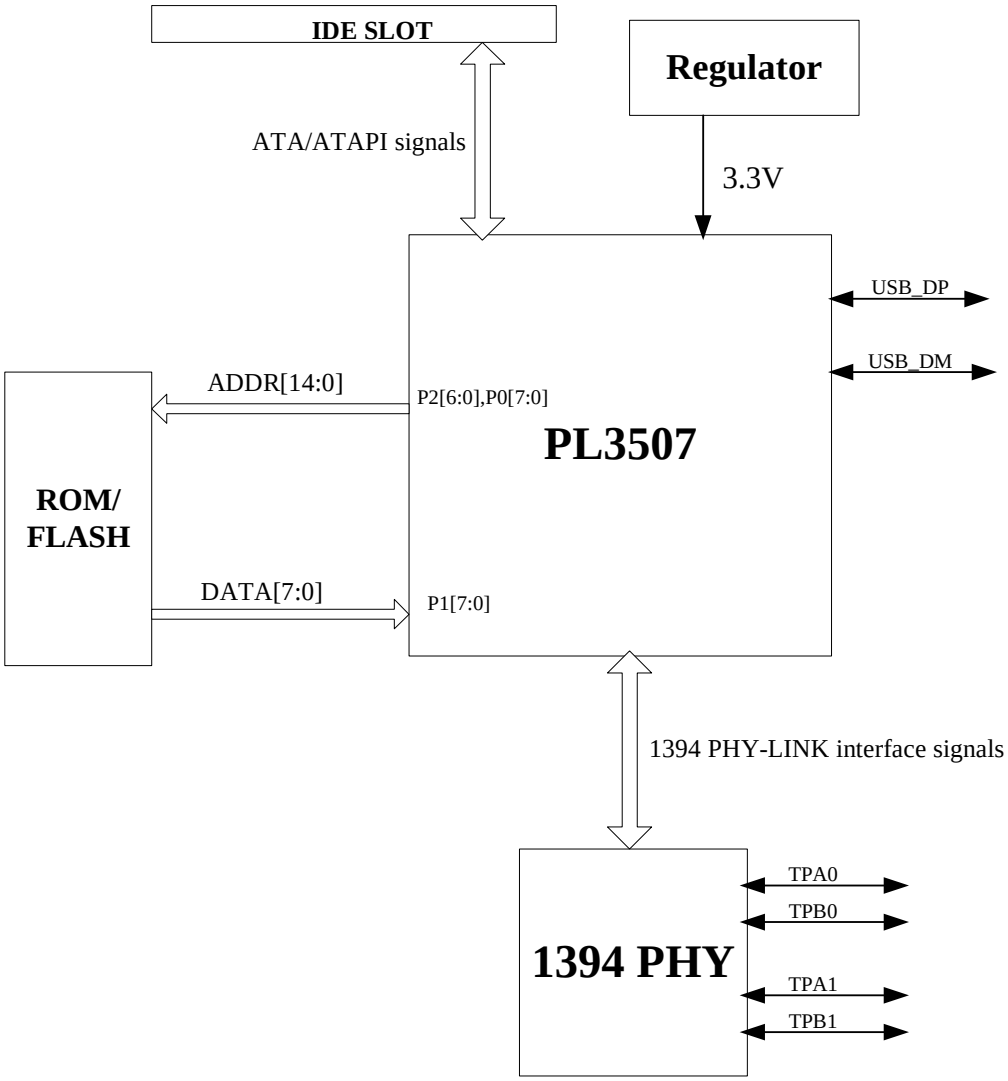


Figure 1-2 System Application Diagram of PL-3507

5.0 Pin Assignment Outline

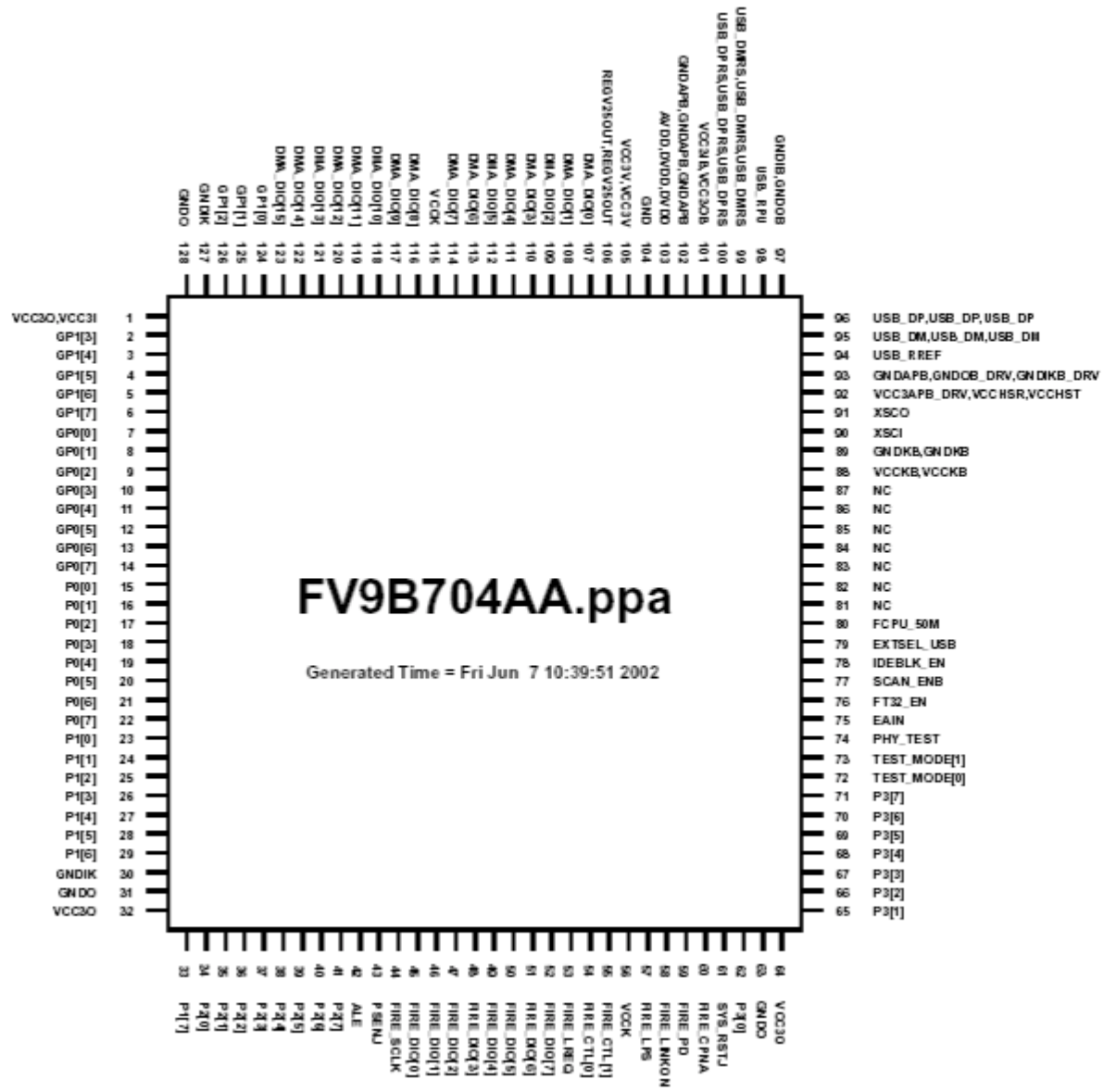


Figure 1-3 Pin Assignment Outline of PL-3507

6.0 PIN Assignment & Description

6.1 GPIO (ATA / ATAPI Interface)

Name	No.	I/O	Description
GP1[0] (IDERSTJ)	124	I/O (O)	Reset signal of ATA/ATAPI devices.
GP1[1]: (DIOWJ) : (STOP)	125	I/O (O)	For modes other than ultra DMA burst in/out, this is a write strobe signal. For ultra DMA burst in/out, host can use this signal to stop ultra DMA burst transfer.
GP1[2]: (DIORJ) : (HDMARDYN) : (HSSTROBE)	126	I/O (O)	For modes other than ultra DMA burst in/out, this is a read strobe signal. For ultra DMA data in burst, it is asserted by host to indicate to the device that the host is ready to accept ultra DMA burst in data. For ultra DMA data out burst, this signal is a data strobe signal from host.
GP1[3] (DMACKJ)	2	I/O (O)	DMA acknowledge to ATA/ATAPI devices.
GP1[4]: (IORDY) : (DDMADRDYN) : (DSTROBE)	3	I/O (I)	For PIO mode 3 and above, this signal is negated to extend the transfer cycle of any host ATA register access. For ultra DMA data out burst, it is asserted by ATA device to indicate to the host that the device is ready to accept ultra DMA burst out data. For ultra DMA data in burst, this signal is a data strobe signal from device.
GP1[5] (INTRQ)	4	I/O (I)	ATA/ATAPI interrupt request.
GP1[6] (DMARQ)	5	I/O (I)	DMA request from ATA/ATAPI devices.
GP1[7]	6	I/O	
GP0[0] (DA0)	7	I/O (O)	Device address bus, used by host to access a register or data port in the storage device.
GP0[1] (DA1)	8	I/O (O)	Device address bus, used by host to access a register or data port in the storage device.
GP0[2] (DA2)	9	I/O (O)	Device address bus, used by host to access a register or data port in the storage device.
GP0[3] (CSJ0)	10	I/O (O)	Chip select signal from host, used to select the command block registers.
GP0[4] (CSJ1)	11	I/O (O)	Chip select signal from host, used to select the control block registers.
GP0[5] (RWAKEJ)	12	I/O	USB remote wakeup.
GP0[6]	13	I/O	
GP0[7] (USBVCC)	14	I/O	USBVCC input through a 100-ohm resistor.
DMA_DIO[0:7]	107~114	I/O	Bidirection data bus between the host and storage device.
DMA_DIO[8:15]	116~123	I/O	Bidirection data bus between the host and storage device.

6.2 1394 PHY-Link Interface

Name	No.	I/O	Description
FIRE_CTL[0:1]	54~55	I/O	1394 PHY-LINK control bus.
FIRE_DIO[0:7]	45~52	I/O	1394 PHY-LINK data bus.
FIRE_LREQ	53	O	1394 Link layer request indicator.
FIRE_SCLK	44	I	1394 System clock supplied by PHY. 49.152Mhz
FIRE_LPS	57	O	1394 Link power status.
FIRE_LINKON	58	I	1394 Link power on request signal from PHY
FIRE_PD	59	O	Power down 1394 PHY.
FIRE_CPNA	60	I	Cable power status input from 1394 PHY.

6.3 Micro Controller Interface

Name	No.	I/O	Description
P0[0:7] (ROM_ADDR[0:7])	15~22	I/O (O)	Port 0 or External ROM/FLASH address bus [0:7].
P2[0:6] (ROM_ADDR[8:14])	34~40	I/O (O)	Port 2[0:6] or External ROM/FLASH address bus [8:14].
P2[7] (ROM_OEJ)	41	I/O (O)	Port 2[7] or External ROM/FLASH output enable signal, active low,
P1[0:7]	23~29, 33	I/O (I)	Port 1 or External ROM/FLASH data input bus.
P3[0:7]	62, 65~71	I/O	Port 3
ALE	42	I/O	Micro-controller Address latch enable signal.
PSENJ	43	I/O	Micro-controller Program storage enable signal.
EAIN	75	I	Micro-controller external access signal.

6.4 USB Interface

Name	No.	I/O	Description
USB_DP	96	I/O	USB 2.0 data pin Data+.
USB_DM	95	I/O	USB 2.0 data pin Data-
USB_RREF	94	I	Connects to external resistor.
USB_RPU	98	I	Connects to external resistor.
USB_DPRS	100	I/O	USB 1.1 data pin Data+, connects to external resistor
USB_DMRS	99	I/O	USB 1.1 data pin Data-, connects to external resistor.
XSCI	90	I	Crystal oscillator input (12 MHz)
XSCO	91	O	Crystal oscillator output (12 MHz)

6.5 Miscellaneous

Name	No.	I/O	Description
SYS_RSTJ	61	I	Reset signal, active low.
TEST_MODE[0:1]	72~73	I	00: Normal operation mode 01: USB PHY module scan test mode. 10: 8032 functional test mode. 11: 8032 scan test mode.
PHY_TEST	74	I	USB PHY test mode.
FT32_EN	76	I	1: internal 8032 enable. 0: internal 8032 disable, use external micro-controller.
SCAN_ENB	77	I	Scan enable signal for scan test modes.
IDEBLK_EN	78	I	1: ATA/ATAPI block enable. 0: PDMA block enable.
EXTSEL_USB	79	I	1: Select USB as active device. 0: Select 1394 as active device.
FCPU_50M	80	I	1: Select 50MHz as CPU clock when 1394 is active. 0: Select 25MHz as CPU clock when 1394 is active.
No Connections	81 ~ 87		

6.6 Regulator

Name	No.	I/O	Description
REG_25VOUT	106	O	Regulator 2.5 Volt output
REG_VCC	105	I	Regulator 3.3 Volt input.
REG_GND	104	I	Regulator ground.

6.7 Power/Ground Pins

Name	No.	I/O	Description
VDD25	56,115	I	2.5 Volt input for core logic.
USB_VDD25	88	I	2.5 Volt input for USB PHY logic.
VCC33	1,32,64	I	3.3 Volt input for pad cells.
USB_VCC33	92, 101, 103	I	3.3 Volt input for USB PHY.
GND	30, 31, 63, 89, 127, 128	I	Digital ground pins.
AGND	93, 97, 102		Analog ground pins for USB PHY.

7.0 General Function Description

The PL-3507 can be used as a USB to ATA/ATAPI or 1394 to ATA/ATAPI bridges for connecting host computers to storage devices like Hard Disk, CDR, CDRW, CDROM, DVDROM and DVDWR. The PL-3507 has auto-detect capability to provide connections either from USB to ATA/ATAPI or 1394 to ATA/ATAPI devices. When both of them are detected, software can select any one of them as active device.

External program storage devices are used, which are shadowing into internal program SRAM during power on or active device switching, the instruction codes of "USB " and "1394" reside in address location "0000h~3fffh" and "4000h~7fffh" separately in the external program devices. At the power on moment, active device is determined by the state of input pin "EXTSEL_USB", if it's logic one, the first 16k byte instruction codes of external program memory will be loaded into internal program memory, otherwise second 16k byte will be loaded. When active device is switching due to USB or 1394 connection status change, the corresponding instruction code will be loaded into internal program memory before reset ends. Only one interface (USB or 1394) can be active at a time to be used for transferring data between host computer and ATA/ATAPI devices. When both two interfaces are connected to host computer, firmware can make a decision to select which interface as active device. The connection detection of both two interfaces are through cable power from USB cable and 1394 cable, when connection status changes, interrupts will happen via INT1 to inform firmware. If both two interfaces (USB and 1394) are connected, firmware should make a decision to select either USB or 1394 as a active device, non-active device should be turned off to prevent confliction.

When connecting to host computers through 1394 cable, host will read configuration ROM from the PL-3507 to recognize the device as a SBP2 storage device, then the host will send login request packets via management ORBs to complete login process. After login finished, the host computers can start to transfer data to/from ATA/ATAPI devices through the PL-3507 by command ORB packets. The PL-3507 has built in a SBP2 hardware engine, which can enhance data transfer rate up to 36 Mbytes/sec.

When connecting to host computers through USB cable, host computer will get device descriptor from the PL-3507 to recognize the device as a mass storage class device, and then host can start to transfer data to/from ATA/ATAPI devices through the PL-3507.

8.0 DC Characteristics

8.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	2.5V Power Supply	-0.3 to 3.0	V
	3.3V Power Supply	-0.3 to 3.9	
V_{IN3}	Input Voltage of 3.3V I/O	-0.3 to V_{cc3} +0.3	V
	Input Voltage of 3.3V I/O with 5V Tolerance	-0.3 to 5.5	
T_{STG}	Storage Temperature	-40 to 150 (TBD)	^{o}C

8.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{DD25}, USB_V_{DD25}	Core Power Supply	2.25	2.5	2.75	V
V_{CC33}	Power Supply of 3.3V I/O	3.0	3.3	3.6	V
USB_V_{CC33}	Power Supply of USB PHY	3.0	3.3	3.6	V
REG_V_{CC}	Power Supply of Regulator	3.0	3.3	3.6	V
REG_25V_{OUT}	Power Supply of Regulator	2.25	2.5	2.75	V
VIN_3	Input Voltage of 3.3V I/O	0	3.3	3.6	V
	Input Voltage of 3.3V I/O with 5V Tolerance	0	3.3	5.25	
T_J	Commercial Junction Operating Temperature	0	25	115	^{o}C

8.3 Leakage Current and Capacitance

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input Leakage Current	No pull-up or pull-down	-10		10	uA
I_{OZ}	Tri-state Leakage Current		-10		10	uA
C_{IN}	Input Capacitance			3.1		pF
C_{OUT}	Output Capacitance			3.1		pF
C_{BID}	Bi-directional Buffer Capacitance			3.1		pF

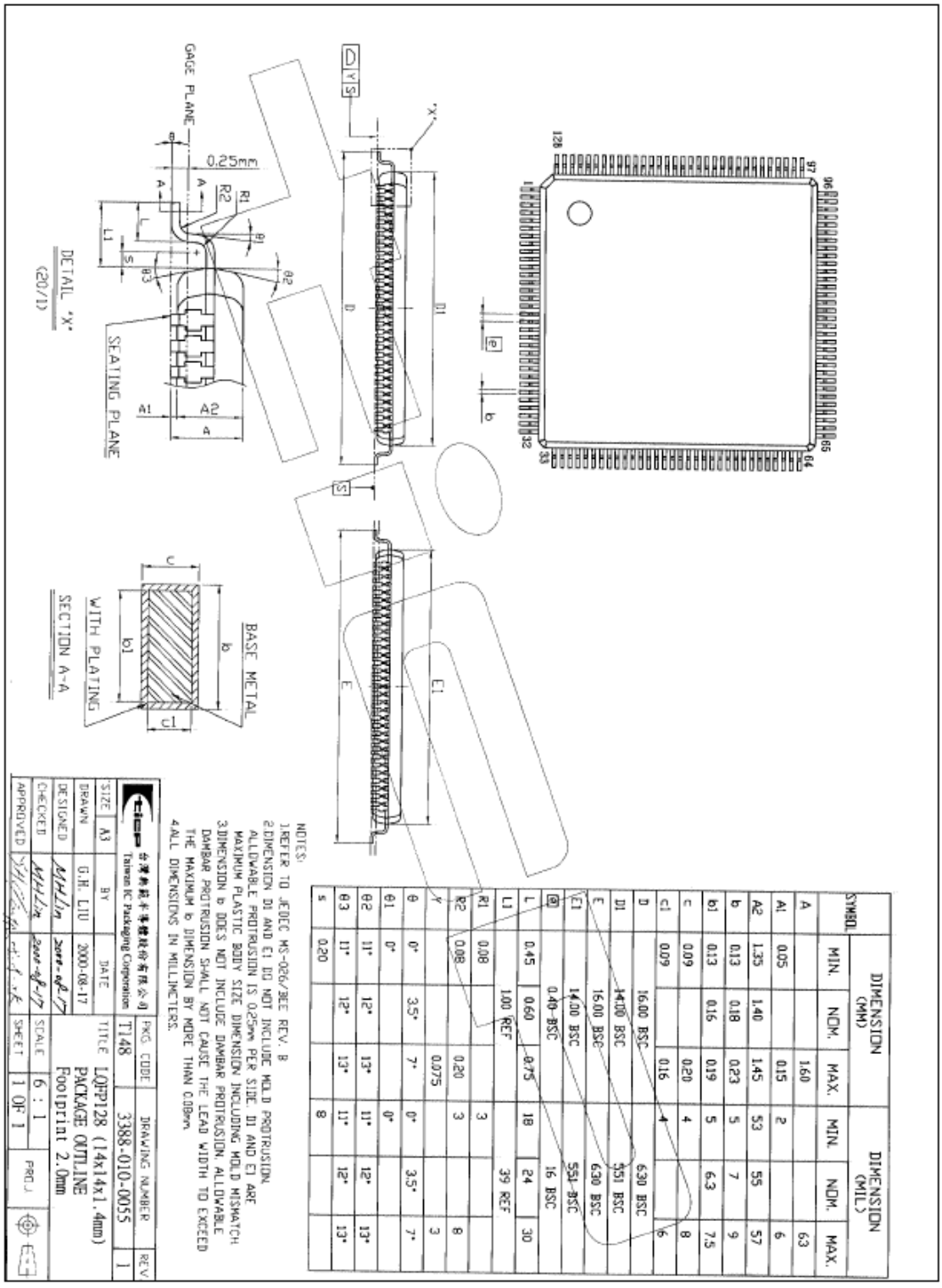
Note: The capacitances listed above do not include PAD capacitance. One can estimate pin capacitance by adding pad's capacitance that is about 0.1 pf and the package capacitance.

8.4 Recommended Ranges of Supply Voltage and Operating Junction Temperature

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNITS
V_{IL}	Input Low Voltage	CMOS/LVTTL			0.8	V
V_{IH}	Input High Voltage	CMOS/LVTTL	2.0			V
V_T	Switching Threshold	CMOS/LVTTL		1.5		V
V_{T-}	Schmitt trigger negative going threshold voltage	CMOS/LVTTL	0.8	1.1		V
V_{T+}	Schmitt trigger positive going threshold voltage	CMOS/LVTTL		1.6	2.0	V
V_{OL}	Output Low Voltage	IOL=2,4…16 mA			0.4	V
V_{OH}	Output High Voltage	IOL=2,4…16 mA	2.4			V
R_{PU}/ R_{PD}	Input Pull-up/down resistance		40	75	190	

9.0 Outline Diagram

9.1 LQ128 Package



SYMBOL	DIMENSION (MM) MIN.	NOM.	MAX.	DIMENSION (MIL) MIN.	NOM.	MAX.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.13	0.18	0.23	5	7	9
b1	0.13	0.16	0.19	5	6.3	7.5
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D		16.00 BSC			630 BSC	
D1		14.00 BSC			551 BSC	
E		16.00 BSC			630 BSC	
E1		14.00 BSC			551 BSC	
e		0.40 BSC			16 BSC	
L	0.45	0.60	0.75	18	24	30
L1		1.00 REF			39 REF	
R1	0.08			3		
R2	0.08		0.20	3		8
y			0.075			3
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
s	0.20			8		

Figure 1-4 Outline Diagram of PL-3507 LQFP128