X3T10/855D

revision 15a

draft proposed American National Standard
Information Technology -

SCSI-3 Parallel Interface

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Dedication

This standard is dedicated to the memory of D.W. (Bill) Spence, who chaired the SPI working group and was a key contributor to this standard.

Mr. Spence had a Master's Degree in Electrical Engineering from Syracuse University with supplemental graduate training in transmission lines. For the past seven years, Mr. Spence had been the Principal Member of X3T9.2 SCSI Committee from Texas Instruments Computer Systems Division. He was also responsible for various aspects of SCSI host adapters and tape drive engineering. Mr. Spence authored many reports and proposals to the X3T9.2 Committee.

There has been a Bill Spence Memorial Scholarship Fund established in Bill's memory. Those interested can contact First National Bank in Eldorado, Texas 76936.

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Abstract

This standard defines mechanical, electrical, and timing requirements for the SCSI-3 Parallel Interface. This standard is principally intended to be used in conjunction with the SCSI-3 Interlocked Protocol Standard. Alternatively, the SCSI-3 Generic Packetized Protocol (GPP) may be used in conjunction with this standard. The resulting interface facilitates the interconnection of computers and intelligent peripherals and thus provides a common interface specification for both systems integrators and suppliers of intelligent peripherals.

Patent Statement

The developers of this standard have requested that holder's of patents that may be required for the implementation of the standard, disclose such patents to the publisher. However neither the developers nor the publisher have undertaken a patent search in order to identify which if any patents may apply to this standard.

As of the date of publication of this standard and following calls for the identification of patents that may be required for the implementation of this standard, no such claims have been made. No further patent search is conducted by the developer or publisher in respect to any standard it processes. No representation is made or implied that license are not required to avoid infringement in the use of this standard.

Document Status

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Foreword

The SCSI protocol is designed to provide efficient peer-to-peer I/O bus devices with up to 8, 16, or 32 devices depending upon the data path widths implemented, including one or more hosts. Data may be transferred asynchronously at rates that depend primarily on device implementation and cable length. Synchronous data transfers are supported at rates up to 10 megatransfers per second. Three data path widths are allowed, 8-bit, 16-bit, and 32-bit. The corresponding maximum transfer rates are 10 megabytes per second, 20 megabytes per second, and 40 megabytes per second.

With any technical document there may arise questions of interpretation as new products are implemented. The X3 Committee has established procedures to issue technical opinions concerning the standards developed by the X3 organization. These procedures may result in SCSI Technical Information Bulletins being published by X3.

These Bulletins, while reflecting the opinion of the Technical Committee that developed the standard, are intended solely as supplementary information to other users of the standard. This standard, ANS X3.***-199x, as approved through the publication and voting procedures of the American National Standards Institute, is not altered by these Bulletins. Any subsequent revisions to this standard may or may not reflect the contents of the Technical Information Bulletins.

Current X3 practice is to make Technical Information Bulletins available through: Global Engineering, 15 Inverness Way East, Englewood, CO 80112-5704. Telephone: (303)792-2181 or (800)854-7179. Facsimile: (303)792-2192.

Introduction

The SCSI-3 Parallel (SPI) Interface standard is divided into eight major clauses:

Clause 1 is the scope.
Clause 2 enumerates the normative references that apply to this standard.
Clause 3 describes the definitions, symbols, and abbreviations used in this standard.
Clause 4 describes the overview (i.e., model of SPI) and the conventions used in this standard.
Clause 5 describes the connectors.
Clause 6 describes the cable characteristics.
Clause 7 describes the electrical characteristics.
Clause 8 describes the SCSI bus signals.
Clause 9 describes the bus timing.
Clause 10 describes the services provided.
Annexes A and B form an integral part of this International Standard. Annexes C to H are for information purposes only.

1 Scope

This standard defines the mechanical, electrical, and timing requirements of the SCSI-3 Parallel Interface to allow conforming devices to inter-operate at the data transport level. The SCSI-3 Parallel Interface is a local I/O bus that can be operated over a wide range of data rates. The objectives of the SCSI-3 Parallel Interface and SCSI-3 Interlocked Protocol are

a) To provide host computers with device independence within a class of devices. Thus, different disk drives, tape drives, printers, optical media drives, and other devices can be added to the host computers without requiring modifications to generic system hardware. Provision is made for the addition of special features and functions through the use of vendor-specific options. Reserved areas are provided for future standardization.

b) To provide compatibility such that properly conforming SCSI-2 devices may interoperate with SCSI-3 devices given that the systems engineering is correctly done. Properly conforming SCSI-2 devices should respond in an acceptable manner to reject SCSI-3 protocol extensions. SCSI-3 protocol extensions are designed to be permissive of such rejections and thus allow the SCSI-2 devices to continue operation without requiring the use of the extension.

The interface protocol includes provision for the connection of multiple initiators (SCSI devices capable of initiating an I/O process) and multiple targets (SCSI devices capable of responding to a request to perform an I/O process). Distributed arbitration (i.e., bus-contention logic) is built into the architecture of SCSI. A priority system awards interface control to the highest priority SCSI device that is contending for use of the bus.

This standard defines the physical attributes of an input/output bus for interconnecting computers and peripheral devices. Figure 1 shows the relationship of this document to other SCSI-3 standards.

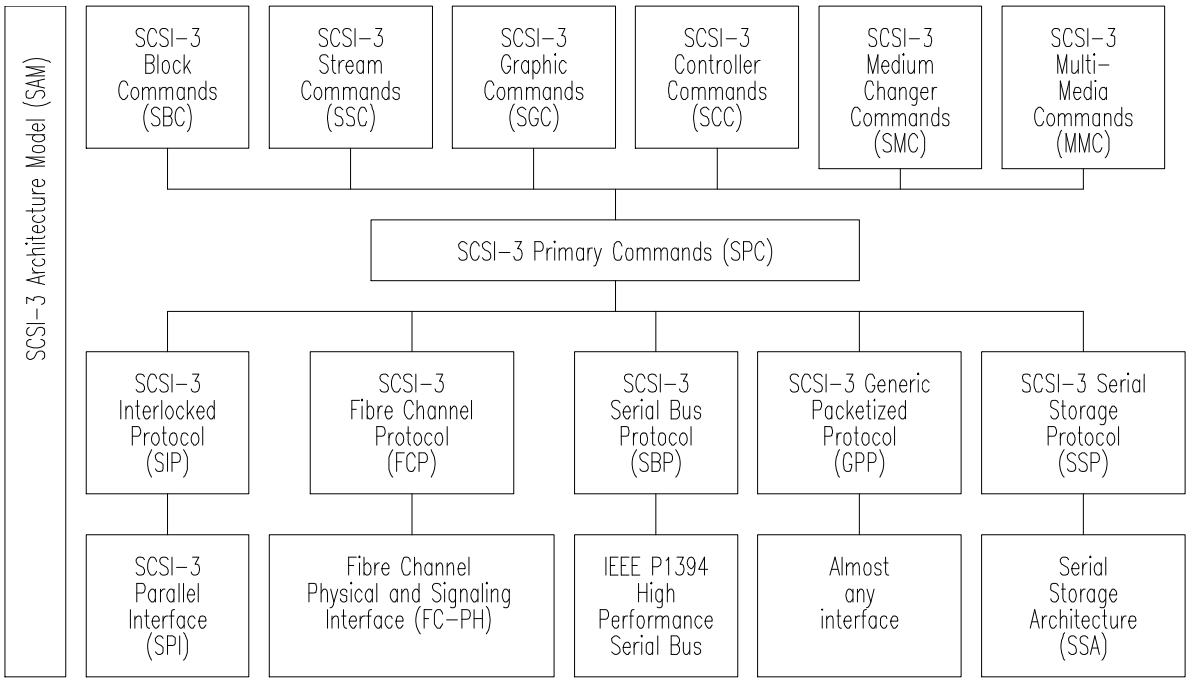


Figure 1 — SCSI-3 Document Roadmap

The roadmap in figure 1 is intended to show the general applicability of documents to one another.

The term SCSI is used wherever it is not necessary to distinguish between the versions of SCSI. The original Small Computer System Interface standard, X3.131-1986, is referred to herein as SCSI-1. SCSI-1 was revised resulting in the Small Computer System Interface - 2 (X3.131-1994), referred to herein as SCSI-2.

The term SCSI-3 refers collectively to the following documents that fall under the jurisdiction of X3T10:

- SCSI-3 Parallel Interface (SPI) [X3T10/855D]
- SCSI-3 Interlocked Protocol (SIP) [X3T10/856D]
- SCSI-3 Fiber Channel Protocol (FCP) [X3T10/993D]
- SCSI-3 Serial Bus Protocol (SBP) [X3T10/992D]
- SCSI-3 Generic Packetized Protocol (GPP) [X3T10/991D]
- SCSI-3 Architecture Model (SAM) [X3T10/994D]
- SCSI-3 Primary Commands (SPC) [X3T10/995D]
- SCSI-3 Block Commands (SBC) [X3T10/996D]
- SCSI-3 Stream Commands (SSC) [X3T10/997D]
- SCSI-3 Graphic Commands (SGC) [X3T10/998D]
- SCSI-3 Medium Changer Commands (SMC) [X3T10/999D]

2 Normative references

The following standards contain provisions which, through reference in this text, constitute provisions of this International Standard. At the time of publication, the editions indicated were valid. The Standards are subject to revision, and parties to agreements based on this International Standard are encouraged to investigate the possibility of applying the most recent editions of the standards indicated below. Members of IEC and ISO maintain registers of currently valid International Standards.

ANSI Y14.5M-1982, *Dimensioning and tolerancing*

ANSI/EIA 364-23A-1985, *Low-level contact resistance test procedure for electronic connectors*

ASTM B827:1992, *Standard practice for conducting mixed flowing gas (MFG) environmental tests* [1]

ASTM D-4566:1990, *Standard test methods for electrical performance properties of Insulations and Jackets for Telecommunications Wire and Cable* [1]

EIA/TIA RS-485-1985, *Electrical Characteristics of Generators and Receivers for use in Balanced Digital Multipoint Systems* [2]

> Note 1 - An implementation that uses differential transceivers is intended for use in conjunction with EIA/TIA RS-485.

ISO 8482:1987, *Information processing systems - Data communication - Twisted pair multipoint interconnections*

ISO/ FEC DIS 10288, *Information technology - Enhanced small computer system interface*

ANSI X3.131-1994, *Small Computer System Interface-2*

---

1. *Available from ASTM, 1916 Race Street, Philadelphia, PA. 19103.*
2. *Available from the Electronic Industries Association, 2001 Eye Street NW, Washington, D.C. 20006.*

3 Definitions, symbols and abbreviations

3.1 Definitions

For the purposes of this standard, the following definitions apply.

3.1.1 A cable. A 50-conductor cable that provides an 8-bit DATA BUS and control signals. The connectors used with this cable are defined in SCSI-2.

3.1.2 P cable. A 68-conductor cable that provides the primary 16-bit DATA BUS and control signals. The connector used with this cable is defined in this standard.

3.1.3 Q cable. A 68-conductor cable that provides the secondary 16-bit DATA BUS. This cable is used in conjunction with the P cable to provide a 32-bit data path. The connector used with this cable is the same as the P cable.

3.1.4 ACKx. A bus signal that is either the ACK or ACKQ signal.

3.1.5 asynch transfer. An information transfer that uses the asynchronous REQ/ACK handshake.

3.1.6 byte. An 8-bit construct.

3.1.7 confirmation. The last step of a confirmed service informing the upper protocol layer that the requested service has been completed.

3.1.8 contact. The electrically-conductive portion of a connector associated with a single conductor in a cable.

3.1.9 DATA BUS. An 8-bit,16-bit or 32-bit DATA BUS (see Section 8.1).

3.1.10 differential. A signalling alternative that employs differential drivers and receivers to improve signal-to-noise ratios and increase maximum cable lengths (also see 3.1.31 single-ended).

3.1.11 fast transfer. A fast synchronous data transfer.

3.1.12 indication. The second step of a service which occurs as a result of a request.

3.1.13 initiator. An SCSI device (usually a host system) that requests an I/O process to be performed by another SCSI device (a target).

3.1.14 initiator role. The mode of operation of a port in which the port performs initiator functions.

3.1.15 mandatory. The referenced item is required to claim conformance with this standard.

3.1.16 megatransfers per second. The repetitive rate at which words of data are transferred across the bus. This is equivalent to megabytes per second on an 8-bit wide bus.

3.1.17 odd parity. Odd logical parity, where the parity bit is driven and verified to be that value that makes the number of assertions on the associated data byte plus the parity bit equal to an odd number (1, 3, 5, or 7). See 3.1.19, parity bit.

3.1.18 optional. The referenced item is not required to claim conformance with this standard, but if the item is implemented it shall conform to the definitions within this standard.

3.1.19 parity bit. A bit associated with a byte that is used to detect the presence of single-bit errors within the byte. The parity bit is driven such that the number of logical ones in the byte plus the parity bit is odd.

3.1.20 port. A single attachment to an SCSI bus from an SCSI device.

3.1.21 REQx. A bus signal that is either the REQ or REQQ signal.

3.1.22 request. the first step of a service.

3.1.23 reserved. The term used for bits, fields, signals, and code values that are set aside for use in future standards.

3.1.24 response. The third step of a confirmed service in reply to an indication.

3.1.25 SCSI address. The decimal representation of the unique address assigned to an SCSI device.

3.1.26 SCSI ID. The bit-significant representation of the SCSI address.

3.1.27 SCSI device. An initiator or a target that can be attached to the SCSI bus.

3.1.28 signal assertion. The act of driving a signal to the true state.

3.1.29 signal negation. The act of performing a signal release or of driving a signal to the false state.

3.1.30 signal release. The act of allowing the cable terminators to bias the signal to the false state (by placing the driver in the high impedance condition).

3.1.31 single-ended. A signalling alternative that employs single-ended drivers and receivers to increase circuit density (also see 3.1.10, differential).

3.1.32 slow transfer. A slow synchronous data transfer.

3.1.33 source (a signal). The act of either signal assertion, signal negation, or signal release.

3.1.34 target. An SCSI device that performs an I/O process requested by an initiator.

3.1.35 target role. The mode of operation of a port in which the port performs target functions.

3.1.36 transceiver. A device that implements both the SCSI bus receiver and transmitter functions.

3.1.37 upper layer protocol. Any protocol that uses the services of the SPI layer.

3.1.38 word. In this standard, this term indicates a 1-byte, 2-byte, or 4-byte construct.

3.2 Symbols and abbreviations

AWG American Wire Gauge

EMC Electro-magnetic compatibility

ESD Electro-static discharge

SCSI Either SCSI-2 or SCSI-3.

SCSI-2 Small Computer System Interface - 2

ULP Upper layer protocol

PIA Parallel interface agent

4 General

4.1 Overview

The SCSI-3 Parallel Interface (SPI) defines the cables, connectors, signals, and transceivers used to interconnect SCSI devices and the services provided to the upper layer protocol.

This standard defines behaviour in terms of functional layers, service interfaces between layers and peer-to-peer protocols. Services are either confirmed services or unconfirmed services. A confirmed service consists of a service request, indication, response, and confirmation. An unconfirmed service consists of only a service request and results in one or more service indications.

Figure 2 shows the service and protocol interactions for a confirmed service.

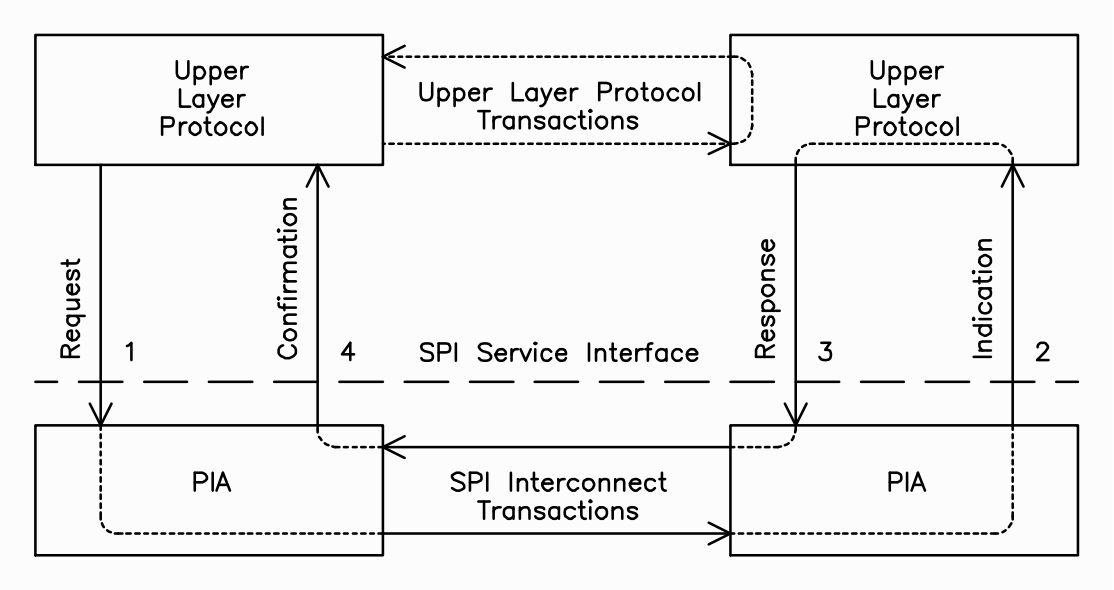


Figure 2 — Model for confirmed services

The SPI service interface consists of the following interactions:

a) A request to the PIA, invoking a service;
b) An indication from the PIA notifying the ULP of an event;
c) A response from the ULP in reply to an indication;
d) A confirmation from the PIA upon service completion.

Figure 3 shows the service and protocol interactions for an unconfirmed service.

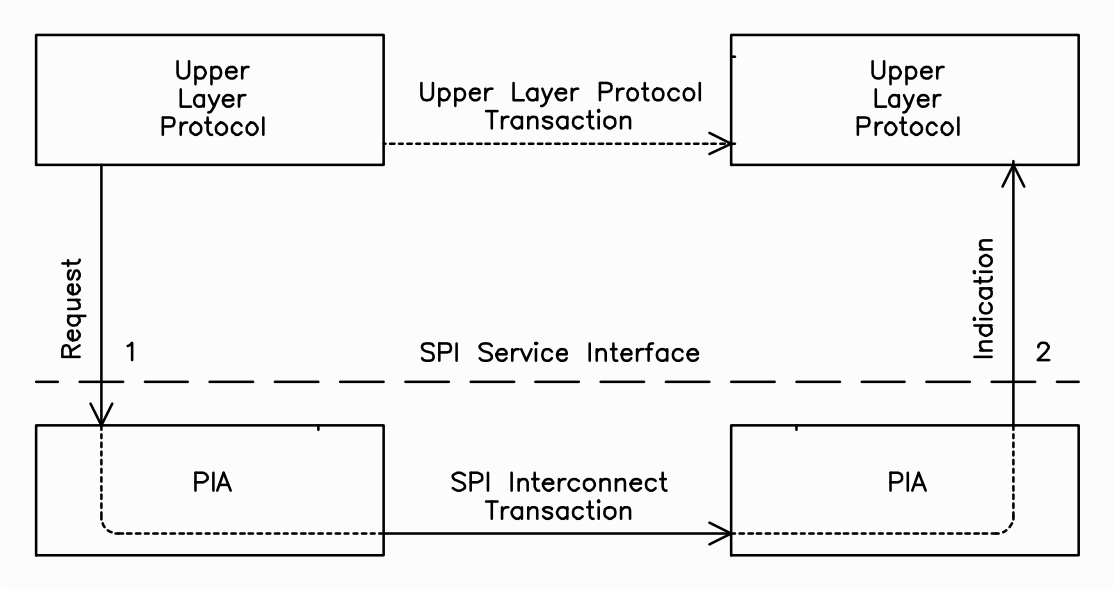


Figure 3 — Model for unconfirmed service

This service consists of the following interactions:

a) A request to the SPI layer, invoking an SPI service;

b) An indication from the SPI layer notifying the upper level protocol of an event.

Clause 10 describes the services provided by SPI to the upper layer protocol.

SPI does not have responsibility for the content or sequencing of phases. SPI is responsible for the correct signal timing on the SCSI bus.

> Note 2 - It may be helpful to envision the PIA as a state machine that implements the services described in this clause. However, the layering of SCSI and the subsequent descriptions are not intended to dictate an actual implementation. It is expected that some portions of the PIA will be implemented in hardware due to the timing requirements, but the standard does not require any particular implementation.

SPI defaults to 8-bit asynch transfer. The 8-bit asynch information transfer mode is always used for all information transfers except DATA IN and DATA OUT. DATA IN and DATA OUT may use asynch, slow, or fast transfers that can be 8-bits, 16-bits or 32-bits wide, if a synchronous transfer agreement or a wide transfer agreement is in effect. SPI may be implemented with either 50- or 68-pin connectors.

4.2 Conventions

Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in the glossary or in the text where they first appear. Names of signals and phases are in all upper-case. Lower-case is used for words having the normal English meaning.

Fields containing only one bit are usually referred to as the "name" bit instead of the "name" field.

Numbers that are not immediately followed by lower-case "b" or "h" are decimal values.

Numbers immediately followed by lower-case "b" (xxb) are binary values.

Numbers immediately followed by lower-case "h" (xxh) are hexadecimal values.

5 SCSI parallel interface connectors

Two types of connectors are defined: nonshielded and shielded. The nonshielded connectors are typically used within an enclosure. The shielded connectors are typically used for external applications where electromagnetic compatibility (EMC) and electrostatic discharge (ESD) protection may be required. Either type of connector may be used with the single-ended or differential transceivers.

The connector shall be a multi-wipe design with contact geometry and normal force sufficient to pass the following test:

a) Measure contact resistances of the connectors being evaluated using a test procedure for low-level contact resistance. Use EIA 364-23A (low-level contact resistance test procedure for electronic connectors) as a reference procedure. Record measurements as initial contact resistances.
b) Mate and un-mate connectors 50 cycles.
c) Contact resistance is measured in accordance with item a) above (this is an optional step).
d) Expose mated connectors to mixed flowing gas consisting of 10 parts per billion (ppb) of chlorine, 10 ppb of hydrogen sulfide, 200 ppb of sulfur dioxide, and 200 ppb of nitrogen dioxide for 20 days at 70 % relative humidity and 30 ^{o}C. Use ASTM B827 (standard practice for conducting mixed flowing gas environmental tests) as a reference procedure.
e) Remove connectors from the mixed flowing gas, remeasure contact resistance in accordance with item a) above, Any contact with an increase of 15 milliohms or greater is a failure.

The resistance shall be measured using a four-point dry-circuit method directly across the mated contact.

5.1 Nonshielded connector

The wide nonshielded SCSI-3 device connector shall be a 68-conductor connector consisting of two rows of 34 female contacts with adjacent contacts 1,27 mm (0,05 in) apart, as shown in figure 4. The non-mating portion of the connector is shown for reference only.

The wide nonshielded mating connector shall be a 68-conductor connector consisting of two rows of 34 male contacts with adjacent contacts 1,27 mm (0,05 in) apart, as shown in figure 5. The non-mating portion of the connector is shown for reference only.

5.2 Shielded connector

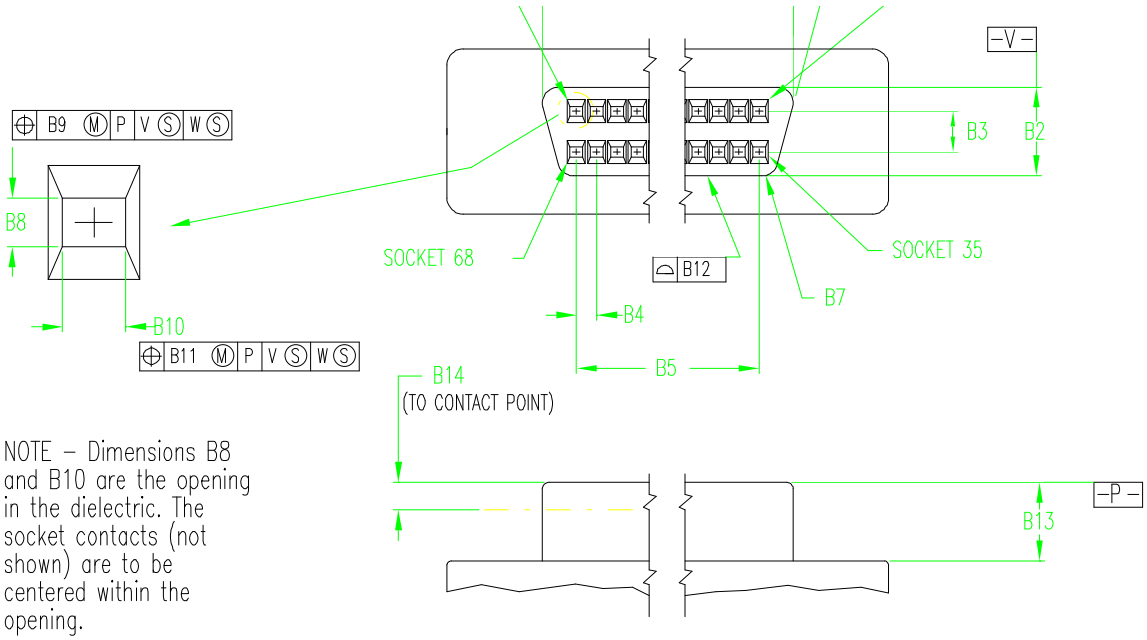
The wide shielded SCSI-3 device connector shall be a 68-conductor connector, consisting of two rows of 34 female contacts with adjacent contacts 1,27 mm (0,05 in) apart, as shown in figure 6. The non-mating portion of the connector is shown for reference only.

The wide shielded mating connector shall be a 68-conductor connector, consisting of two rows of 34 male contacts with adjacent contacts 1,27 mm (0,05 in) apart, as shown in figure 7. The non-mating portion of the connector is shown for reference only.

Cable retention shall consist of 2-56 jack screws capable of withstanding a minimum torque of 1.2 Nm inch-pounds.

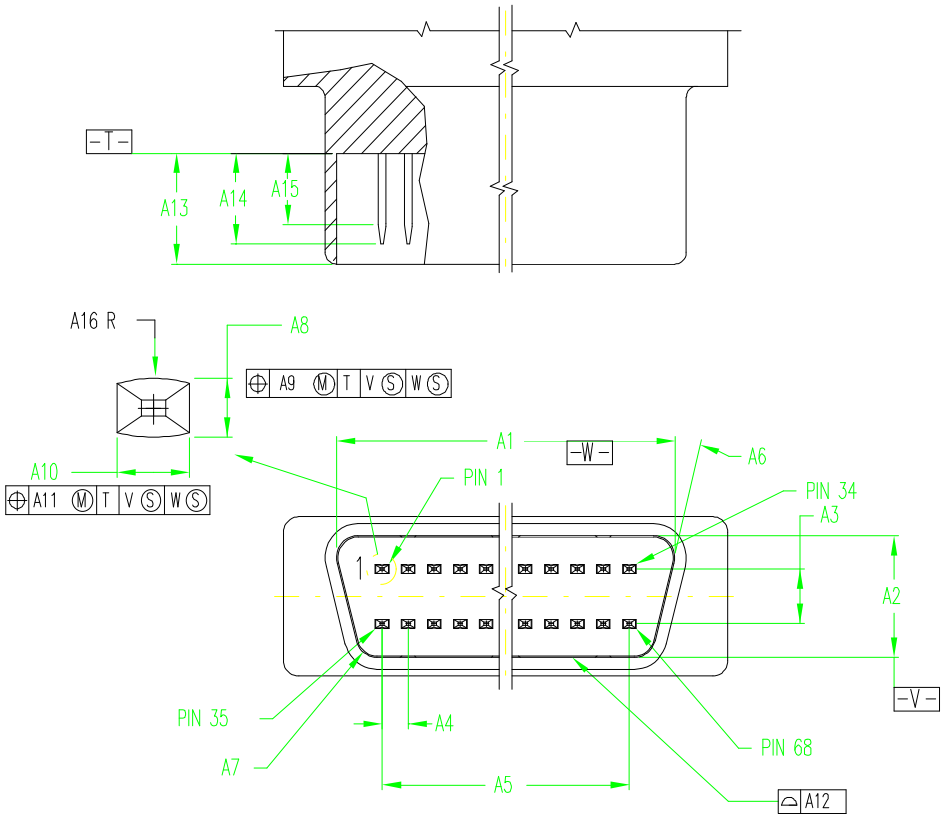
The d.c. resistance from the cable shield where it attaches to the connector to the enclosure should be less than 10 milliohms.

> Note 3 - In order to support daisy-chain connections, SCSI devices that use shielded connectors should provide two shielded device connectors on the device enclosure. Inside the enclosure the cable should be looped from one shielded connector to the other. The loop passes the connecting point to the transceivers within the enclosure in such a manner that stub lengths are minimized. The length of the cable within the device enclosure is included when calculating the total cable length of the SCSI bus.



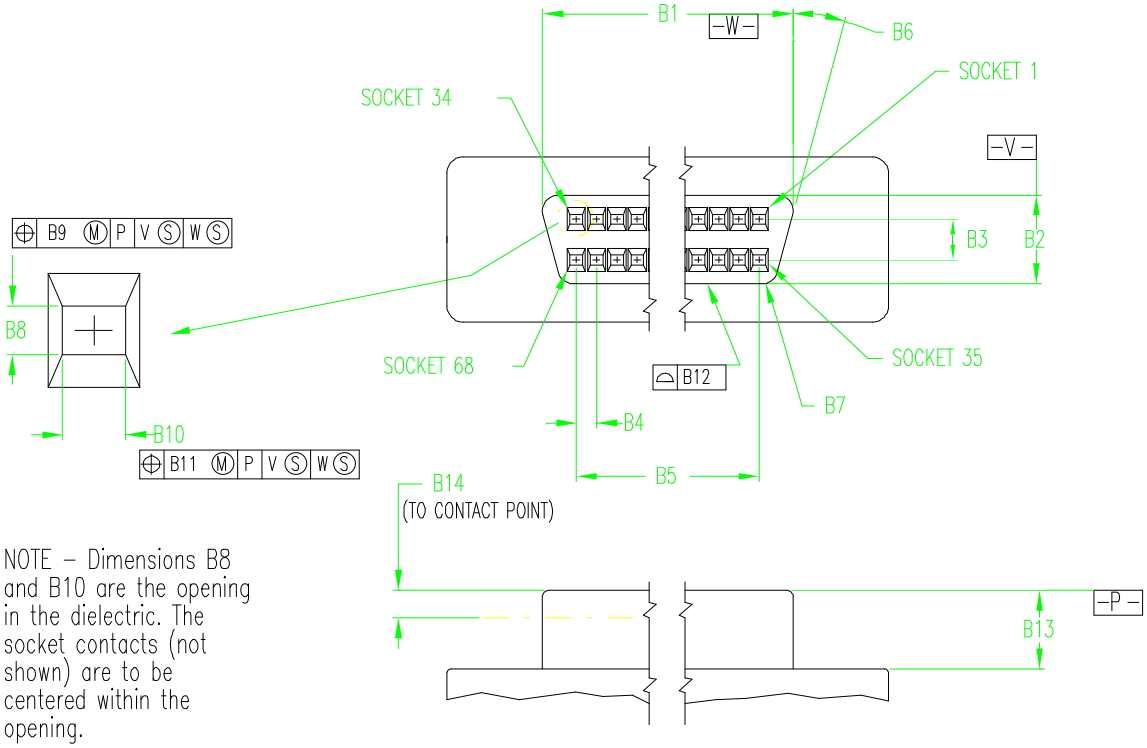
Dimensions	68 Position	
	Millimeters	Inches
B1	46,13	1,816
B2	5,54	0,218
B3	2,54	0,100
B4	1,27	0,050
B5	41,91	1,650
B6	15 °	15
B7	1,00 R	0,039 R
B8	0,61±0,05	0,024±0,002
B9	0,15	0,006
B10	0,86±0,10	0,034±0,004
B11	0,15	0,006
B12	0,05	0,002
B13	5,00±0,13	0,197±0,005
B14	1,75 MAX	0,069 MAX

Figure 4 — Nonsielded device connector



Dimensions	68 Position	
	Millimeters	Inches
A1	46,28	1,822
A2	5,69	0,224
A3	2,54	0,100
A4	1,27	0,050
A5	41,91	1,650
A6	15 °	15 °
A7	1,04 R	0,041 R
A8	0,396±0,010	0,0156±0,0004
A9	0,23	0,009
A10	0,60±0,03	0,024±0,001
A11	0,23	0,009
A12	0,05	0,002
A13	5,15±0,15	0,203±0,006
A14	4,39 MAX	0,173 MAX
A15	3,02 MIN	0,119 MIN
A16	1,02±0,25	0,040±0,010

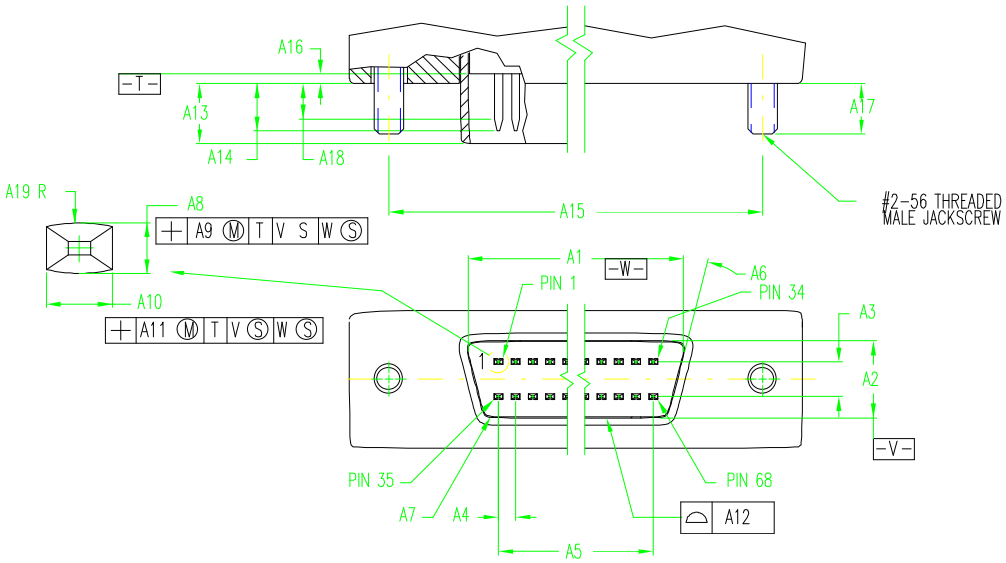
Figure 5 — Nonsielded mating connector



NOTE – Dimensions B8 and B10 are the opening in the dielectric. The socket contacts (not shown) are to be centered within the opening.

Dimensions	68 Position	
	Millimeters	Inches
B1	46,13	1,816
B2	5,54	0,218
B3	2,54	0,100
B4	1,27	0,050
B5	41,91	1,650
B6	15 °	15
B7	1,00 R	0,039 R
B8	0,61±0,05	0,024±0,002
B9	0,15	0,006
B10	0,86±0,10	0,034±0,004
B11	0,15	0,006
B12	0,05	0,002
B13	5,00±0,13	0,197±0,005
B14	1,75 MAX	0,069 MAX

Figure 6 — Shielded device connector



Dimensions	Millimeters	Inches
A1	46,28	1,822
A2	5,69	0,224
A3	2,54	0,100
A4	1,27	0,050
A5	41,91	1,650
A6	15°	15°
A7	1,04 R	0,041 R
A8	0,396±0,010	0,0156±0,0004
A9	0,23	0,009
A10	0,60±0,03	0,024±0,001
A11	0,23	0,009
A12	0,05	0,002
A13	4,90±0,10	0,193±0,004
A14	4,27 max.	0,168 max.
A15	57,91±0,13	2,280±0,005
A16	0,25±0,13	0,010±0,005
A17	3,43±0,15	0,135±0,006
A18	2,64 min.	0,104 min.
A19	1,02±0,25	0,040±0,010

Figure 7 — Shielded mating connector

5.3 Connector contact assignments

The connector contact assignments are defined in 5.3.1 and 5.3.2. The signals are defined in 8.1. The items under singal name labeld TERMPWR, TERMPWRQ, and RESERVED are not signals and are not required to meet the cable characteristics for signals in clause 6.1. See 6.2 for characteristics of TERMPWR and TERMPWRQ. See 6.3 for characteristics of RESERVED lines.

5.3.1 Single-ended assignments

Table 1 defines the connector contact assignments to a primary SCSI bus that uses single-ended transceivers.

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Table 1 — Connector contact assignments for the single-ended primary bus

Signal name	Connector contact number	SCSI bus conductor number	SCSI bus conductor number	Connector contact number	Signal name
GROUND	1	1	2	35	-DB(12)
GROUND	2	3	4	36	-DB(13)
GROUND	3	5	6	37	-DB(14)
GROUND	4	7	8	38	-DB(15)
GROUND	5	9	10	39	-DB(P1)
GROUND	6	11	12	40	-DB(0)
GROUND	7	13	14	41	-DB(1)
GROUND	8	15	16	42	-DB(2)
GROUND	9	17	18	43	-DB(3)
GROUND	10	19	20	44	-DB(4)
GROUND	11	21	22	45	-DB(5)
GROUND	12	23	24	46	-DB(6)
GROUND	13	25	26	47	-DB(7)
GROUND	14	27	28	48	-DB(P)
GROUND	15	29	30	49	GROUND
GROUND	16	31	32	50	GROUND
TERMPWR	17	33	34	51	TERMPWR
TERMPWR	18	35	36	52	TERMPWR
RESERVED	19	37	38	53	RESERVED
GROUND	20	39	40	54	GROUND
GROUND	21	41	42	55	-ATN
GROUND	22	43	44	56	GROUND
GROUND	23	45	46	57	-BSY
GROUND	24	47	48	58	-ACK
GROUND	25	49	50	59	-RST
GROUND	26	51	52	60	-MSG
GROUND	27	53	54	61	-SEL
GROUND	28	55	56	62	-C/D
GROUND	29	57	58	63	-REQ
GROUND	30	59	60	64	-I/O
GROUND	31	61	62	65	-DB(8)
GROUND	32	63	64	66	-DB(9)
GROUND	33	65	66	67	-DB(10)
GROUND	34	67	68	68	-DB(11)

NOTES
1 The minus sign next to a signal indicates active low.
2 The conductor number refers to the conductor position when using 0,635 mm (0,025 in) centerline flat-ribbon cable.

Table 2 defines the connector contact assignments to a secondary SCSI bus that uses single-ended transceivers.

Table 2 — Connector contact assignments for the single-ended secondary bus

Signal name	Connector contact number	SCSI bus conductor number	SCSI bus conductor number	Connector contact number	Signal name
GROUND	1	1	2	35	-DB(28)
GROUND	2	3	4	36	-DB(29)
GROUND	3	5	6	37	-DB(30)
GROUND	4	7	8	38	-DB(31)
GROUND	5	9	10	39	-DB(P3)
GROUND	6	11	12	40	-DB(16)
GROUND	7	13	14	41	-DB(17)
GROUND	8	15	16	42	-DB(18)
GROUND	9	17	18	43	-DB(19)
GROUND	10	19	20	44	-DB(20)
GROUND	11	21	22	45	-DB(21)
GROUND	12	23	24	46	-DB(22)
GROUND	13	25	26	47	-DB(23)
GROUND	14	27	28	48	-DB(P2)
GROUND	15	29	30	49	GROUND
GROUND	16	31	32	50	GROUND
TERMPWRQ	17	33	34	51	TERMPWRQ
TERMPWRQ	18	35	36	52	TERMPWRQ
RESERVED	19	37	38	53	RESERVED
GROUND	20	39	40	54	GROUND
GROUND	21	41	42	55	TERMINATED
GROUND	22	43	44	56	GROUND
GROUND	23	45	46	57	TERMINATED
GROUND	24	47	48	58	-ACKQ
GROUND	25	49	50	59	TERMINATED
GROUND	26	51	52	60	TERMINATED
GROUND	27	53	54	61	TERMINATED
GROUND	28	55	56	62	TERMINATED
GROUND	29	57	58	63	-REQQ
GROUND	30	59	60	64	TERMINATED
GROUND	31	61	62	65	-DB(24)
GROUND	32	63	64	66	-DB(25)
GROUND	33	65	66	67	-DB(26)
GROUND	34	67	68	68	-DB(27)

NOTES
1 The minus sign next to a signal indicates active low.
2 The conductor number refers to the conductor position when using 0,635 mm (0,025) in centerline flat-ribbon cable.

5.3.2 Differential connector contact assignments

Table 3 defines the connector contact assignments to a primary SCSI bus that uses differential transceivers.

Table 3 — Connector contact assignments for the differential primary bus

Signal name	Connector contact number	SCSI bus conductor number	SCSI bus conductor number	Connector contact number	Signal name
+DB(12)	1	1	2	35	-DB(12)
+DB(13)	2	3	4	36	-DB(13)
+DB(14)	3	5	6	37	-DB(14)
+DB(15)	4	7	8	38	-DB(15)
+DB(P1)	5	9	10	39	-DB(P1)
GROUND	6	11	12	40	GROUND
+DB(0)	7	13	14	41	-DB(0)
+DB(1)	8	15	16	42	-DB(1)
+DB(2)	9	17	18	43	-DB(2)
+DB(3)	10	19	20	44	-DB(3)
+DB(4)	11	21	22	45	-DB(4)
+DB(5)	12	23	24	46	-DB(5)
+DB(6)	13	25	26	47	-DB(6)
+DB(7)	14	27	28	48	-DB(7)
+DB(P)	15	29	30	49	-DB(P)
DIFFSENS	16	31	32	50	GROUND
TERMPWR	17	33	34	51	TERMPWR
TERMPWR	18	35	36	52	TERMPWR
RESERVED	19	37	38	53	RESERVED
+ATN	20	39	40	54	-ATN
GROUND	21	41	42	55	GROUND
+BSY	22	43	44	56	-BSY
+ACK	23	45	46	57	-ACK
+RST	24	47	48	58	-RST
+MSG	25	49	50	59	-MSG
+SEL	26	51	52	60	-SEL
+C/D	27	53	54	61	-C/D
+REQ	28	55	56	62	-REQ
+I/O	29	57	58	63	-I/O
GROUND	30	59	60	64	GROUND
+DB(8)	31	61	62	65	-DB(8)
+DB(9)	32	63	64	66	-DB(9)
+DB(10)	33	65	66	67	-DB(10)
+DB(11)	34	67	68	68	-DB(11)

NOTES
1 The minus sign next to a signal indicates active low.
2 The conductor number refers to the conductor position when using 0,635 mm (0,025 in) centerline flat-ribbon cable.

Table 4 defines the connector contact assignments to a secondary SCSI bus that uses differential transceivers

Table 4 — Connector contact assignments for the differential secondary bus

Signal name	Connector contact number	SCSI bus conductor number	SCSI bus conductor number	Connector contact number	Signal name
+DB(28)	1	1	2	35	-DB(28)
+DB(29)	2	3	4	36	-DB(29)
+DB(30)	3	5	6	37	-DB(30)
+DB(31)	4	7	8	38	-DB(31)
+DB(P3)	5	9	10	39	-DB(P3)
GROUND	6	11	12	40	GROUND
+DB(16)	7	13	14	41	-DB(16)
+DB(17)	8	15	16	42	-DB(17)
+DB(18)	9	17	18	43	-DB(18)
+DB(19)	10	19	20	44	-DB(19)
+DB(20)	11	21	22	45	-DB(20)
+DB(21)	12	23	24	46	-DB(21)
+DB(22)	13	25	26	47	-DB(22)
+DB(23)	14	27	28	48	-DB(23)
+DB(P2)	15	29	30	49	-DB(P2)
DIFFSENS	16	31	32	50	GROUND
TERMPWRQ	17	33	34	51	TERMPWRQ
TERMPWRQ	18	35	36	52	TERMPWRQ
RESERVED	19	37	38	53	RESERVED
TERMINATED	20	39	40	54	TERMINATED
GROUND	21	41	42	55	GROUND
TERMINATED	22	43	44	56	TERMINATED
+ACKQ	23	45	46	57	-ACKQ
TERMINATED	24	47	48	58	TERMINATED
TERMINATED	25	49	50	59	TERMINATED
TERMINATED	26	51	52	60	TERMINATED
TERMINATED	27	53	54	61	TERMINATED
+REQQ	28	55	56	62	-REQQ
TERMINATED	29	57	58	63	TERMINATED
GROUND	30	59	60	64	GROUND
+DB(24)	31	61	62	65	-DB(24)
+DB(25)	32	63	64	66	-DB(25)
+DB(26)	33	65	66	67	-DB(26)
+DB(27)	34	67	68	68	-DB(27)

NOTES
1 The minus sign next to a signal indicates active low.
2 The conductor number refers to the conductor position when using 0,635 mm (0,025 in) centerline flat-ribbon cable.

6 SCSI bus cables

This clause defines the characteristics of cables used to connect SCSI-3 parallel interface devices. These cables are part of the SCSI bus. The length of the cable within the device enclosure is included when calculating the total cable length of the SCSI bus. The four types of cables allowed are:

a) unshielded flat-ribbon cable;
b) unshielded flat twisted-pair ribbon cable;
c) unshielded round twisted-pair cables;
d) shielded round twisted-pair cables.

If twisted-pair cables are used, the twisted pairs in the cable shall be wired to physically opposing contacts in the connector.

The items under signal name labelled TERMPWR, TERMPWRQ, and RESERVED are not signals and are not required to meet the cable characteristics for signals in 6.1. See 6.2 for characteristics of TERMPWR and TERMPWRQ. See 6.3 for characteristics of RESERVED lines.

Interconnection of SCSI devices by means other than cables is allowed (e.g., by backplanes using printed wiring boards). Detailed descriptions of these other means are not part of this standard, however, all segments of an SCSI bus are subject to the electromagnetic concepts presented in this standard. These are:

a) characteristic impedance (see Table 5);
b) propagation delay (see Table 6);
c) cumulative length;
d) stub length; and
e) device spacing (see 6.4 and 6.5).

A primary SCSI-3 bus carries a 16-bit data bus and the signals used to provide the services specified in clause 10. A primary SCSI-3 bus provides an 8-bit or 16-bit data transfer path. A secondary SCSI-3 bus carries an additional 16-bit data bus that, used in conjunction with a primary SCSI-3 bus, provides a 32-bit data transfer path. The same cable and connector assembly can be used for both the primary and secondary SCSI-3 buses.

Note 4 - A primary SCSI-2 bus carries an 8-bit data bus and the signals used to provide the services specified in clause 10. A primary SCSI-2 bus provides an 8-bit data path. A secondary SCSI-2 bus carries an additional 24-bit data bus that, used in conjunction with a primary SCSI-2 bus, provides a 32-bit data path.

6.1 Cable characteristics for signals

The signals shall not be internally connected together within the connectors or cables. See 8.1 for signal definitions.

The minimum conductor size for signals should be 0,050 92 mm^2 (30 AWG).

The characteristic impedance of the cable is defined in table 5. Two measurement techniques can be used to determine the impedance. The single-ended measurement technique is applicable to cables used with single-ended transceivers. The differential measurement technique is applicable to cables used with differential transceivers. See annex D for measurement techniques.

Table 5 — Characteristic impedance of cable

Description	Single-ended measurement technique (ohms)	Differential measurement technique (ohms)
Maximum, any signal	96	160
Nominal, any signal	84	122
Minimum, any signal	72	115
Maximum difference between any two signals in the same cable	12	20

The propagation delay of SCSI cables is defined in table 6.

Table 6 — Propagation delay of cables

Description	Value (ns/m)
Maximum, any signal	5,4
Maximum difference between any two signals on the same cable	0,15

The maximum signal attenuation for round cables shall be 0,095 dB maximum per meter at 5 Mhz, measured differentially.

6.2 Cable characteristics for TERMPWR and TERMPWRQ lines

The minimum conductor size for the TERMPWR and TERMPWRQ lines should be 0,050 92 mm^2 (30 AWG) for 68-conductor cables.

The minimum conductor size for the TERMPWR line should be 0,080 98 mm^2 (28 AWG) for 50-conductor cables that support a single TERMPWR line.

The TERMPWR and TERMPWRQ lines should be decoupled at each terminator with at least a 2,2 uF bypass capacitor and a 0,01 uF high-frequency capacitor.

See 7.3 for additional information.

6.3 Cable characteristics for RESERVED lines

The RESERVED lines shall be left open in the bus terminator assemblies and in the SCSI devices. The RESERVED lines shall have continuity from one end of the SCSI bus to the other end.

The minimum conductor size should be 0,050 92 mm^2 (30 AWG).

6.4 Cables used with single-ended transceivers

The maximum cumulative cable length when using single-ended transceivers should be 3 m. Implementations that limit the transfer rate to a maximum of 5 megatransfers per second may extend the cumulative cable length to 6 m.

The stub length shall not exceed 0,1 m. The stub length is measured from the transceiver to the mainline interconnection. Stubs should be spaced at least 0,3 m apart and stub clustering should be avoided.

The following requirements based on the connector contact assignments in 5.3.1 ensure that all SCSI-3 round cables can be used with either single-ended or differential transceivers:

a) cable conductor pairs #47-48 (ACK) and #57-58 (REQ) shall be in the cable core;
b) if there are more than three conductor pairs in the cable core, conductor pairs #47-48 (ACK) and #57-58 (REQ) shall not be adjacent to each other;
c) cable conductor pairs used for the DATA BUS (DBnPx) shall be in the outer layer of the cable;
d) each cable conductor pair shall consist of the ground and its associated signal.

See annex C for information on interconnecting busses of different widths and annex F for terminator, impedance, crosstalk, and bus length considerations.

6.5 Cables used with differential transceivers

Twisted-pair cable (either twisted-flat or discrete wire twisted pairs) should be used with differential transceivers.

The maximum cumulative cable length shall be 25 m.

The stub length shall not exceed 0,2 m. The stub length is measured from the transceiver to the mainline interconnection. Stubs should be spaced at least 0,3 m apart and stub clustering avoided.

7 SCSI parallel interface electrical characteristics

The SCSI-3 parallel interface can use one of the following transceiver alternatives:

a) single-ended drivers and receivers, in which one conductor of each signal pair is active and one is grounded;

b) differential drivers and receivers, in which both conductors of each signal pair are active.

The single-ended and differential alternatives are mutually exclusive.

For measurements in this clause, SCSI bus termination is assumed to be external to the SCSI device. See for the terminating requirements for the RESERVED lines. SCSI devices may have provision for allowing optional internal termination provided the internal termination conforms with or when enabled and the SCSI device, including the disabled termination, conforms with or when the internal termination is disabled.

7.1 Single-ended alternative

7.1.1 Single-ended termination

All SCSI bus signals are common among all devices connected to the bus. All signal lines shall be terminated at both ends with a terminator that is compatible with the type of transceivers used in the SCSI devices. The termination points define the ends of the bus. These termination points may be internal to an SCSI device.

Note 5 - If the termination is provided within an SCSI device that device should not be removed from the SCSI bus while the bus is in use.

All single-ended signals not defined as RESERVED, GROUND, or TERMPWR shall be terminated exactly once at each end of the bus. The termination of each signal shall meet the following requirements:

a) the terminators shall be powered by the TERMPWR line and may receive additional power from other sources but shall not require such additional power for proper operation (see 6.3);

b) each terminator shall source current to the signal line whenever its terminal voltage is below 2,5 V d.c. and this current shall not exceed 24 mA for any line voltage above 0,2 V d.c.;

c) the voltage on all released signal lines shall be at least 2,5 V d.c.;

d) these conditions shall be met with any legal configuration of targets and initiators as long as at least one device is supplying TERMPWR;

e) the terminator at each end of the SCSI bus (see 7.1.4) shall add a maximum of 25 pF capacitance to each signal.

f) the terminator shall not source current to the signal line whenever its terminal voltage is above 3,24 V d.c. except in laptop applications where the bus is less than 0,3 m.

7.1.2 Single-ended output characteristics

Single-ended signals shall use either passive-negation or active-negation drivers. Passive-negation drivers have two states, asserted and high-impedance. Passive-negation drivers are usually implemented using an open-collector or an open-drain circuit. Active-negation drivers have three states: asserted, negated, and high-impedance. Each signal sourced by an SCSI device shall have the following output characteristics when measured at the SCSI device's connector:

a) V_{OL} (low-level output voltage) = 0,0 V d.c. to 0,5 V d.c. at I_{OL} = 48 mA (signal asserted);

b) V_{OH} (high-level output voltage) = 2,5 V d.c. to 5,25 V d.c. (signal negated).

Note 6 - Passive-negation drivers do not source current to achieve the V_{OH} voltage level. They enter the high-impedance state and rely on the terminator to source the current.

Active-negation drivers shall have the following additional output characteristics when measured at the SCSI device's connector:

a) V_{OH} (high-level output voltage) = 2,0 V d.c. to 3,24 V d.c. at I_{OH} = 7 mA (signal negated);

b) V_{OH} (high-level output voltage) < 3,0 V d.c. at I_{OH} = 20 mA (signal negated).

Note 7 - In words, these expressions mean: If the driver is negated and loaded at 7 mA, then the output voltage is between 2,0 V d.c. and 3,24 V d.c. If the current is 20 mA, the voltage is less than 3,0 V d.c.

Note 8 - It is recommended that drivers not source current above 4,0 V d.c..

While active-negation drivers may be used on any non-OR-tied signal (see 8.2), their usage is particularly valuable on the ACK, REQ, ACKQ, and REQQ signals, because these signals are vulnerable to double clocking on the true-to-false transition. Additional benefit may be achieved by using active-negation drivers on the DATA BUS and parity signals when operating in fast synchronous data transfer mode by reducing the skews between the first group of signals (ACK, REQ, ACKQ, and REQQ) and the DATA BUS and parity signals.

All single-ended drivers shall maintain the high-impedance state during power-on and power-off cycles.

SCSI devices should meet the following specifications for all signals:

a) t_{rise} (rise time) = 5 ns min (10 % to 90 % of full amplitude);

b) t_{fall} (fall time) = 5 ns min (90 % to 10 % of full amplitude).

The recommended test circuit for measurement of rise time is shown in figure 8.

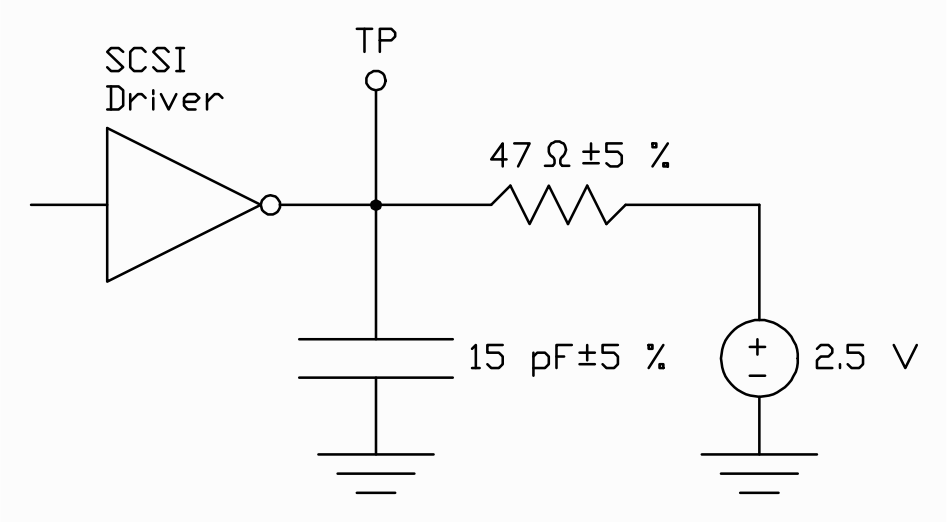


Figure 8 — Rise time test circuit

7.1.3 Single-ended input characteristics

SCSI devices with power-on shall meet the following electrical characteristics on each signal (including both receivers and disabled drivers):

a) V_{IL} (Low-level input voltage) = 0,0 V d.c. to 0,8 V d.c. (signal true);

b) V_{IH} (High-level input voltage) = 2,0 V d.c. to 5,25 V d.c. (signal false);

c) I_{IL} (Low-level input current) = +/- 20 uA at V_I = 0,5 V d.c.;

d) I_{IH} (High-level input current) = +/- 20 uA at V_I = 2,7 V d.c.;

e) Minimum input hysteresis = 0,3 V d.c.

The transient leakage current that may occur (e.g. with some ESD protection circuits) at the time of physical insertion of an SCSI device is an exponentially decaying current that does not exceed the following specifications:

a) $I_{IH.HP}$ (hot-plug high-level input current peak value excluding the first 10ns) = + 1.5 mA at V_I = 2.7 V d.c.;

b) T_{HP} (transient current duration to 10 % of peak value) = 20 μs maximum.

SCSI devices with power-off should meet the above I_{IL} and I_{IH} electrical characteristics on each signal, except at time of physical insertion, when $I_{IH,HP}$ and T_{HP} prevail.

The nominal switching threshold should be 1,4 V d.c. to achieve maximum noise immunity and to ensure proper operation with complex cable configurations.

The REQ/REQQ and ACK/ACKQ receivers, after recognizing a negation transition, shall not respond to a signal reversal for at least 10 ns.

7.1.4 Single-ended input and output characteristics

The single-ended signals shall have the following characteristics when measured at the SCSI device's connector:

a) I_L (Leakage current) = -20 μA to + 20 μA at V_I = 0,0 V d.c. to 5,25 V d.c. (high-impedance state);

b) Maximum signal capacitance = 25 pF, measured at the beginning of the stub (see annex F).

7.2 Differential alternative

7.2.1 Differential termination

All SCSI bus signals are common among all devices connected to the bus. All signal lines shall be terminated at both ends with a terminator that is compatible with the type of transceivers used in the SCSI devices. The termination points define the ends of the bus. These termination points may be internal to an SCSI device.

Note 9 - If the termination is provided within an SCSI device that device should not be removed from the SCSI bus while the bus is in use.

All differential signals consist of two lines denoted +SIGNAL and -SIGNAL. A signal is true when +SIGNAL is more positive than -SIGNAL, and a signal is false when -SIGNAL is more positive than +SIGNAL. All assigned differential signals described in except TERMPWR, RESERVED, and GROUND shall be terminated at each end of the cable with a terminator network as shown in figure 9. Resistor tolerances in the terminator network shall be ± 5 % or less. The characteristic impedance of differential terminators is 122 ohms.

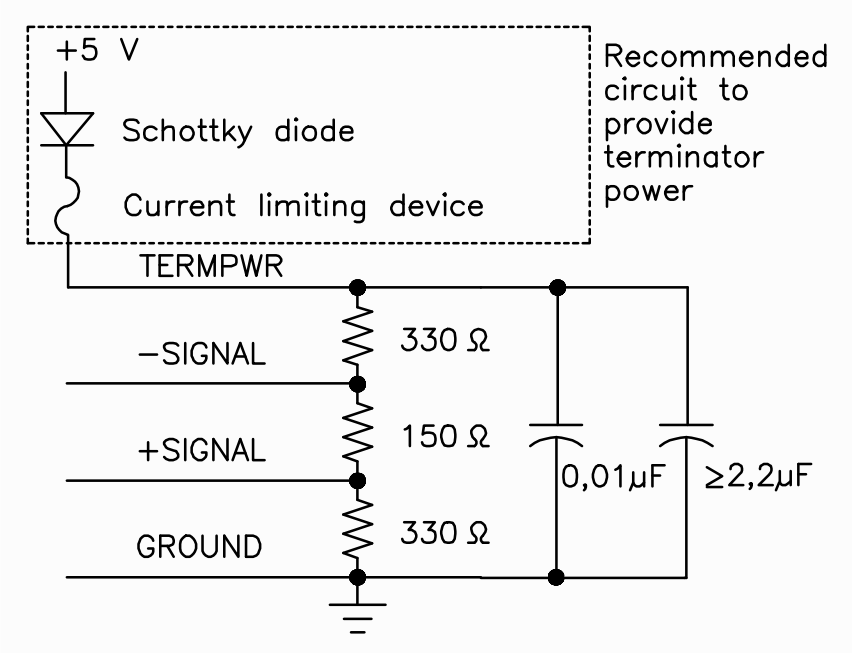


Figure 9 — Termination for differential devices

7.2.2 Differential output characteristics

Each differential signal sourced by an SCSI device shall have the following output characteristic when measured at the SCSI device's connector

a) V_{OD} (differential output voltage) = 1,0 V minimum;
b) shall conform to EIA RS-485 (ISO 8482-1982, TIA TR30.2).

All differential drivers shall maintain the high-output impedance during power-on and power-off cycles.

The test circuit for testing these characteristics is shown in figure 10.

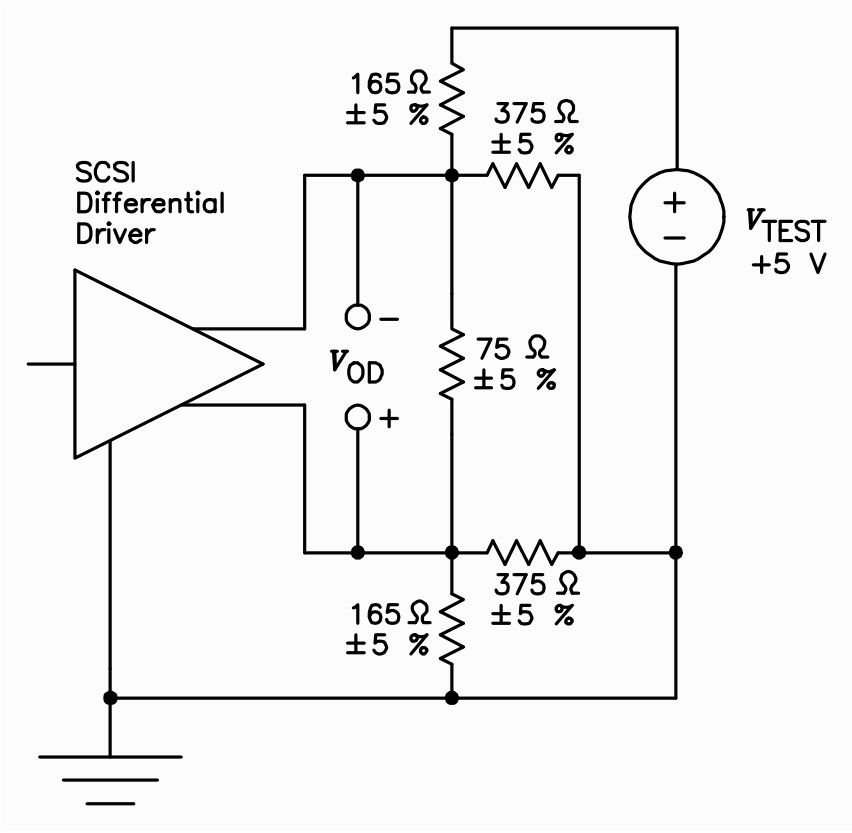


Figure 10 — Differential test circuit

7.2.3 Differential input characteristics

Each differential signal shall have the following characteristics when measured at the SCSI device's connector (including both receivers and disabled drivers):

a) maximum input capacitance = 25 pF;
b) minimum input hysteresis = 35 mV.

The input characteristics shall additionally conform to EIA RS-485 (ISO 8482 TIA TR30.2).

7.2.4 Differential driver protection

The DIFFSENS signal is a single-ended signal that is used as an active high enable for the differential drivers. If a single-ended device or terminator is inadvertently connected, this signal is grounded, disabling the differential drivers (see figure 11).

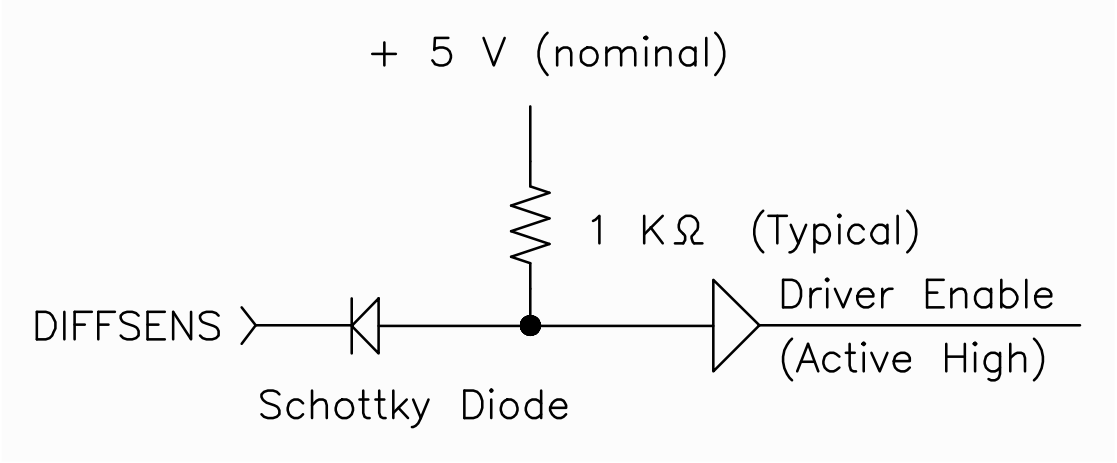


Figure 11 — Differential driver protection circuit

7.3 Terminator power

Provision shall be made to provide power from one or more sources to the TERMPWR lines of the SCSI bus. This power shall be supplied through a low forward drop diode or similar semiconductor that prevents backflow of power if one of the sources of TERMPWR is powered-off.

All terminators independent of location shall be powered from the TERMPWR lines. SCSI devices shall sink no more than 1,0 mA from the TERMPWR lines and no more than 1,0 mA from the TERMPWRQ lines except to power an optional internal terminator.

Regulatory agencies may require limiting maximum (short circuit) current to the TERMPWR lines. These requirements generally mandate the use of current limiting circuits and may restrict the number of sources provided for TERMPWR.

SCSI-3 devices providing TERMPWR shall have the characteristics defined in table 7.

Table 7 — Terminator power characteristics

	TERMPWR voltage (V d.c.) minimum	TERMPWR voltage (V d.c.) maximum	Minimum TERMPWR source current (mA)	Recommended TERMPWR current limiting (A)
Single-ended	4,25	5,25	1 500	2,0
Differential	4,00	5,25	1 000	2,0

Note 10 - SCSI devices connected with a 50-conductor cable that utilizes only one TERMPWR line cannot meet the source current requirements in table 7 unless the TERMPWR conductor size is 0,080 98 mm^2 (28 AWG) minimum.

8 SCSI bus signals

Information transfer on the SCSI bus is allowed between only two SCSI devices at any given time. The maximum number of devices is determined by the width of the data path implemented. The devices can be any combination of initiators (or ports in initiator role) and targets (or ports in target role) provided there is at least one of each.

Each SCSI device has an SCSI address and a corresponding SCSI ID bit assigned to it. When two SCSI devices communicate on the SCSI bus, one acts in an initiator role and the other acts in a target role. The SCSI device in initiator role originates an I/O process and the SCSI device in target role performs the I/O process.

Note 11 - An SCSI device usually has a fixed role as an initiator or target, but some devices may be able to assume either role.

Table 8 shows the relationship between SCSI Addresses, SCSI IDs, and arbitration priority. A hyphen ("-") represents a logical zero bit.

Table 8 — Arbitration priorities by SCSI ID

SCSI address	DB31	DB24	DB23	DB16	DB15	DB8	DB7	DB0	Priority
7	-	-	-	-	-	-	1	-	1
6	-	-	-	-	-	-	-	1	2
5	-	-	-	-	-	-	-	-	3
4	-	-	-	-	-	-	-	-	4
3	-	-	-	-	-	-	-	-	5
2	-	-	-	-	-	-	-	-	6
1	-	-	-	-	-	-	-	-	7
0	-	-	-	-	-	-	-	-	8
15	-	-	-	-	1	-	-	-	9
14	-	-	-	-	-	1	-	-	10
13	-	-	-	-	-	-	-	-	11
12	-	-	-	-	-	-	-	-	12
11	-	-	-	-	-	-	-	-	13
10	-	-	-	-	-	-	-	-	14
9	-	-	-	-	-	-	-	-	15
8	-	-	-	-	-	-	-	-	16
23	-	-	1	-	-	-	-	-	17
22	-	-	-	1	-	-	-	-	18
21	-	-	-	-	1	-	-	-	19
20	-	-	-	-	-	1	-	-	20
19	-	-	-	-	-	-	-	-	21
18	-	-	-	-	-	-	-	-	22
17	-	-	-	-	-	-	-	-	23
16	-	-	-	-	-	-	-	-	24
31	1	-	-	-	-	-	-	-	25
30	-	1	-	-	-	-	-	-	26
29	-	-	1	-	-	-	-	-	27
28	-	-	-	1	-	-	-	-	28
27	-	-	-	-	1	-	-	-	29
26	-	-	-	-	-	1	-	-	30
25	-	-	-	-	-	-	1	-	31
24	-	-	-	-	-	-	-	1	32

8.1 Signal descriptions

BSY (BUSY). An "OR-tied" signal that indicates that the SCSI bus is in use.

SEL (SELECT). An "OR-tied" signal used by an initiator PIA to select a target or by a target PIA to reselect an initiator.

C/D (CONTROL/DATA). A signal sourced by a target PIA that indicates whether control or data information is on the DATA BUS. True indicates CONTROL.

I/O (INPUT/OUTPUT). A signal sourced by a target PIA that controls the direction of data movement on the DATA BUS with respect to an initiator. True indicates INPUT. This signal is also used to distinguish between SELECTION and RESELECTION phases.

MSG (MESSAGE). A signal sourced by a target PIA to indicate the MESSAGE phase. True indicates MESSAGE.

REQ (REQUEST). A signal sourced by a target PIA to indicate a request for an information transfer on the low-order data path.

REQQ (REQUEST). A signal sourced by a target PIA to indicate a request for an information transfer on the high-order data path.

ACK (ACKNOWLEDGE). A signal sourced by an initiator PIA to respond with an acknowledgement of an information transfer on the low-order data path.

ACKQ (ACKNOWLEDGE). A signal sourced by an initiator PIA to respond with an acknowledgement of an information transfer on the high-order data path.

ATN (ATTENTION). A signal sourced by an initiator PIA when the attention flag is set in the request or response that generates the attention flag in the confirmation when asserted.

RST (RESET). An "OR-tied" signal that generates the RESET flag when asserted.

DB(7-0,P) (8-bit DATA BUS). Eight data-bit signals, plus a parity-bit signal that form the 8-bit DATA BUS. DB(P) shall contain odd parity for DB(7-0)). Bit significance and priority during arbitration are shown in table 8.

DB(15-0,P,P1) (16-bit DATA BUS). Sixteen data-bit signals, plus two parity-bit signals that form the 16-bit DATA BUS. DB(P,P1) shall contain odd parity for DB(7-0) and DB(15-8), respectively. Bit significance and priority during arbitration are shown in table 8.

DB(31-0,P,P1,P2,P3) (32-bit DATA BUS). Thirty-two data-bit signals, plus four parity-bit signals that form the 32-bit DATA BUS. DB(P,P1,P2,P3) shall contain odd parity for DB(7-0), DB(15-8), DB(23-16), and DB(31-24), respectively. Bit significance and priority during arbitration are shown in table 8.

8.2 Signal states

Signals may be true (asserted) or false (negated) state. Signals that are asserted are actively driven to the true state. Signals that are negated may either be actively driven to the false state or released to the false state. A signal that is released goes to the false state because the bias of the terminator pulls the signal false. OR-tied signals shall not be actively driven false.

> Note 12 - The advantage of actively negating signals false during information transfer is that the noise margin is higher than if the signal is simply released. This facilitates reliable data transfer at high transfer rates.

Bits of the DATA BUS are defined as one when the signal is true, and defined as zero when the signal is false.

8.3 OR-tied signals

The BSY, SEL, and RST signals shall be OR-tied. Any signal other than BSY, SEL, and RST may employ OR-tied or non-OR-tied drivers.

BSY and RST signals may be simultaneously driven true by several drivers. No signals other than BSY, SEL, RST, and DB(P,P1,P2,P3) are simultaneously driven by two or more drivers. Parity bits shall not be driven false during the ARBITRATION phase but may be driven false in other phases. There is no operational problem in mixing OR-tied and non-OR-tied drivers on signals other than BSY, SEL, and RST.

8.4 Signal sources

Table 9 indicates the type of SCSI device allowed to source each signal. No attempt is made to show if the source is driving asserted, driving negated, or is released. All SCSI device drivers that are not active sources shall be in the high-impedance state. The RST signal may be asserted by any SCSI device at any time.

Table 9 — Signal sources

SCSI bus phase	P cable signals						Q cable signals		
	A cable signals								
	BSY	SEL	C/D I/O MSG REQ	ACK ATN	DB7-0 DB(P)	DB15-8 DB(P1)	REQQ	ACKQ	DB31-16 DB(P2) DB(P3)
BUS FREE	None	None	None	None	None	None	None	None	None
ARBITRATION	All	Win	None	None	S ID	S ID	None	None	S ID
SELECTION	I&T	Init	None	Init	Init	Init	None	None	Init
RESELECTION	I&T	Targ	Targ	Init	Targ	Targ	None	None	Targ
SETUP	Targ	None	Targ	Init	IorT	IorT	None	None	IorT
COMMAND	Targ	None	Targ	Init	Init	None	None	None	None
DATA IN	Targ	None	Targ	Init	Targ	Targ	Targ	Init	Targ
DATA OUT	Targ	None	Targ	Init	Init	Init	Targ	Init	Init
STATUS	Targ	None	Targ	Init	Targ	None	None	None	None
MESSAGE IN	Targ	None	Targ	Init	Targ	None	None	None	None
MESSAGE OUT	Targ	None	Targ	Init	Init	None	None	None	None

All: The signal shall be driven by all SCSI devices that are actively arbitrating.
S ID: A unique data bit (the SCSI ID) shall be driven by each SCSI device that is actively arbitrating; the other data bits shall be released (i.e., not driven) by this SCSI device. The parity bit(s) may be released or driven to the true state, but shall not be driven to the false state during this phase.
I&T: The signal shall be driven by the initiator, target, or both, as specified in the SELECTION phase and RESELECTION phase.
IorT: Initiator or target or neither, depending on the state of the I/O signal and the bus width.
Init: If driven, this signal shall be driven only by the active initiator.
None: The signal shall be released; that is, not driven by any SCSI device. The bias circuitry of the bus terminators pulls the signal to the false state.
Win: The signal shall be driven by the one SCSI device that wins arbitration.
Targ: If the signal is driven, it shall be driven only by the active target.

9 SCSI parallel bus timing

Unless otherwise indicated, the delay-time measurements for each SCSI device, shown in table 10, shall be calculated from signal conditions existing at that SCSI device's port. Thus, these measurements (except cable skew delay) can be made without considering delays in the cable. The timing characteristics of each signal are described in the following paragraphs. The timing specifications in this clause may be applied to SCSI-2 parallel interface.

The transfer period specifies the minimum time allowed between the leading edges of successive REQ pulses and of successive ACK pulses while using synchronous data transfers (see XXX).

Fast data transfers require a negotiated transfer period greater than or equal to 100ns and less than 200ns with a REQ/ACK offset greater than zero. If fast data transfers are agreed upon, fast timing shall be observed even though the actual data transfer period is greater than or equal to 200ns.

Slow data transfers require a negotiated transfer period greater than or equal to 200 ns with a REQ/ACK offset greater than zero.

Asynch information transfers require a REQ/ACK offset of zero. The transfer period does not apply to these information transfers.

Table 10 — SCSI bus timing values

Timing description	Timing values		
	fast	slow	asynch
Arbitration Delay	2,4 µs	2,4 µs	2,4 µs
Bus Clear Delay	800 ns	800 ns	800 ns
Bus Free Delay	800 ns	800 ns	800 ns
Bus Set Delay	1,8 µs	1,8 µs	1,8 µs
Bus Settle Delay	400 ns	400 ns	400 ns
Cable Skew Delay [1]	4 ns	4 ns	4 ns
Data Release Delay	400 ns	400 ns	400 ns
Receive Assertion Period	22 ns	70 ns	n/a
Receive Hold Time [2]	25 ns	25 ns	n/a
Receive Negation Period	22 ns	70 ns	n/a
Receive Setup Time [2]	15 ns	15 ns	n/a
Recieve Period Tolerance	0,5%	0,5%	n/a
Reset Hold Time	25 µs	25 µs	25 µs
Selection Abort Time	200 µs	200 µs	200 µs
Selection Time-out Delay [3]	250 ms	250 ms	250 ms
Deskew Delay	45 ns	45 ns	45 ns
Transmit Assertion Period	30 ns	80 ns	n/a
Transmit Hold Time [2]	33 ns	53 ns	n/a
Transmit Negation Period	30 ns	80 ns	n/a
Transmit Setup Time [2]	23 ns	23 ns	n/a
Transmit Period Tolerance	0,25%	0,25%	n/a

Notes
1 This time does not apply at the SCSI device connectors.
2 See annex E for examples of how to calculate setup and hold timing.
3 This is a recommended time. It is not mandatory.

9.1 Arbitration delay

The minimum time an SCSI device shall wait from asserting the BSY signal for arbitration until the DATA BUS can be examined to see if arbitration has been won. There is no maximum time.

9.2 Bus clear delay

The maximum time for an SCSI device to release all SCSI bus signals after

a) the BUS FREE phase is detected (the BSY and SEL signals are both false for a bus settle delay);
b) the SEL signal is received from another SCSI device during the ARBITRATION phase;
c) the transition of the RST signal to true.

For item a) above, the maximum time for an SCSI device to release all SCSI bus signals is 1 200 ns from the BSY and SEL signals first becoming both false. If an SCSI device requires more than a bus settle delay to detect BUS FREE phase, it shall release all SCSI bus signals within a bus clear delay minus the excess time.

9.3 Bus free delay

The minimum time that an SCSI device shall wait from its detection of the BUS FREE phase (BSY and SEL both false for a bus settle delay) until its assertion of the BSY signal in preparation for entering the ARBITRATION phase.

9.4 Bus set delay

The maximum time for an SCSI device to assert the BSY signal and its SCSI ID after it detects a BUS FREE phase for the purpose of entering the ARBITRATION phase.

9.5 Bus settle delay

The minimum time to wait for the bus to settle after changing certain control signals as called out in the protocol definitions.

9.6 Cable skew delay

The maximum difference in propagation time allowed between any two SCSI bus signals measured between any two SCSI devices.

9.7 Data release delay

The maximum time for an initiator to release the DATA BUS signals following the transition of the I/O signal from false to true.

9.8 Receive assertion period

The minimum time required at a device receiving a REQ or REQQ signal for the signal to be asserted while using synchronous data transfers. Also, the minimum time required at a device receiving an ACK or ACKQ signal for the signal to be asserted while using synchronous data transfers. In single-ended operation, the time period is measured at the 0,8 V level. The timings for the REQQ and ACKQ signals only apply to wide data transfers.

9.9 Receive hold time

The minimum time required at the receiving device between the assertion of the REQ or REQQ signal or the ACK or ACKQ signals and the changing of the DATA BUS while using synchronous data transfers. The timings for the REQQ and ACKQ signals only apply to 32-bit wide data transfers.

9.10 Receive negation period

The minimum time required at a device receiving a REQ or REQQ signal for the signal to be negated while using synchronous data transfers. Also, the minimum time required at a device receiving an ACK or ACKQ signal for the signal to be asserted while using synchronous data transfers. In single-ended operation, the time period is measured at the 2,0 V level. The timings for the REQQ and ACKQ signals only apply to wide data transfers.

9.11 Receive setup time

The minimum time required at the receiving device between the changing of DATA BUS and the assertion of the REQ or REQQ signal or the ACK or ACKQ signal while using synchronous data transfers. The timings for the REQQ and ACKQ signals only apply to 32-bit wide data transfers.

9.12 Receive period tolerance

The minimum tolerance that an SCSI device shall allow to be subtracted from the negotiated synchronous period.

9.13 Reset hold time

The minimum time that the RST signal is asserted. There is no maximum time.

9.14 Selection abort time

The maximum time that an SCSI device shall take from its most recent detection of being selected or reselected until asserting a the BSY signal in response. This time-out is required to ensure that a target or initiator does not assert the BSY signal after a SELECTION or RESELECTION phase has been aborted. This is not the selection time-out period (see 10.3.4 and e) for a complete description)

9.15 Selection time-out delay

The minimum time that an initiator or target should wait for a the assertion of the BSY signal in response during the SELECTION or RESELECTION phase before starting the time-out procedure. Note that this is only a recommended time period.

9.16 System deskew delay

The minimum time that a device should wait after receiving an SCSI signal to ensure that any signals transmitted at the same time are valid.

9.17 Transmit assertion period

The minimum time that a target shall assert the REQ or REQQ signal while using synchronous data transfers. Also, the minimum time that an initiator shall assert the ACK or ACKQ signal while using synchronous data transfers. The timing for the REQQ and ACKQ signals only apply to 32-bit wide data transfers.

9.18 Transmit hold time

The minimum time provided by the transmitting device between the assertion of the REQ or REQQ signal or the ACK or ACKQ signal and the changing of the DATA BUS while using synchronous data transfers. The timings for the REQQ and ACKQ signals only apply to 32-bit wide data transfers.

9.19 Transmit negation period

The minimum time that a target shall negate the REQ or REQQ signal while using synchronous data transfers. Also, the minimum time that an initiator shall negate the ACK or ACKQ signal while using synchronous data transfers. The timing for the REQQ and ACKQ signals only apply to 32-bit wide data transfers.

9.20 Transmit setup time

The minimum time provided by the transmitting device between the changing of DATA BUS and the assertion of the REQ or REQQ signal or the ACK or ACKQ signal while using synchronous data transfers. The timings for the REQQ and ACKQ signals only apply to 32-bit wide data transfers.

9.21 Transmit period tolerance

The maximum tolerance that an SCSI device may subtract from the negotiated synchronous period.

10 SCSI parallel interface services

The SCSI parallel interface transport services are provided by the parallel interface agent (PIA) enabling the upper layer protocol (ULP) to manage the SCSI BUS and accomplish tasks. The transport services are described in terms of the services that the PIA provides.

An upper layer protocol operating in target role may request any service except a selection service. An upper layer protocol operating in initiator role may request only selection and reset services.

10.1 Bus free service

A bus free service is an unconfirmed service used to generate a bus free.

10.1.1 Bus free request

The bus free request contains no parameters.

When a bus free request is received the PIA shall release the BSY and SEL signals, and shall release any other asserted SCSI bus signals within a bus settle delay plus a bus clear delay of the release of the BSY and SEL signals.

10.1.2 Bus free indication

The bus free indication contains no parameters.

The PIA shall generate a bus free indication when the SEL and BSY signals are both continuously false for at least a bus settle delay. The PIA shall continue to generate this indication as long as the SEL and BSY signals remain false.

> Note 13 - This bus settle delay is necessary because a transmission line phenomenon known as a "wire-OR glitch" may cause the BSY signal to briefly appear false, even though it is being asserted.

10.2 Reset service

A reset service is an unconfirmed service used to determine if an SCSI bus reset has occurred. It is also used to generate an SCSI bus reset.

10.2.1 Reset request

A reset request contains no parameters.

When a reset request is received the PIA shall assert the RST signal for a minimum of a reset hold time.

While the RST signal is true, the state of all SCSI bus signals other than the RST signal is not defined. A ULP may request a reset service at any time. The bus free indication always follows the reset service.

10.2.2 Reset indication

A reset indication contains no parameters.

When the RST signal is asserted the PIA shall:

a) release all the SCSI bus signals except the RST signal within a bus clear delay of the transition of the RST signal to true;
b) generate a reset indication.

The bus clear delay following a RST signal transition to true is measured from the original transition of the RST signal, not from the time that the signal was validated. This limits the time to validate the RST signal to a maximum of a bus clear delay.

> Note 14 - Environmental conditions (e.g., static discharge) may generate brief glitches on the RST signal. It is recommended that SCSI devices not react to these glitches. The manner of rejecting glitches is vendor-specific.

10.3 Selection service

The selection service is a confirmed service that combines arbitration with selection. The selection service provides a means to establish an initial connection or reconnection.

10.3.1 Selection request

The selection request contains the SCSI ID of the device to be selected and the attention flag.

When a selection request is received the initiator PIA shall arbitrate for the SCSI bus, and if successful, select the designated SCSI device.

To perform an arbitration the initiator PIA shall:

a) wait until the SEL and BSY signals are both continuously false for at least a bus settle delay;

b) not assert any SCSI BUS signal within a bus free delay of step a)above;

c) assert the BSY signal, assert its SCSI ID, and release all other DATA BUS signals no sooner than a bus free delay and no later than a bus set delay of step a)above;

Note 15 - There is no maximum delay before asserting the BSY signal and the SCSI ID following the bus free delay in step b)above as long as the SEL and BSY signals remain false. However, SCSI devices that delay longer than a bus settle delay plus a bus set delay from the time when the BSY and SEL signals first become false may fail to participate in arbitration when competing with faster SCSI devices.

d) wait at least an arbitration delay (measured from the assertion of the BSY signal) and then examine the DATA BUS to determine which SCSI IDs are true;

e) If a higher priority SCSI ID exists on the DATA BUS, then arbitration has been lost. The initiator PIA shall release the BSY signal and the SCSI ID within a bus clear delay after the SEL signal becomes true. The initiator PIA proceeds to selection confirmation (see 10.3.4);

f) If a higher priority SCSI ID does not exist on the DATA BUS then arbitration has been won (See table 8). The initiator PIA shall assert the SEL signal. It shall not change any signals until at least a bus clear delay plus a bus settle delay has elapsed after asserting the SEL signal. The initiator PIA proceeds to selection.

To perform a selection the initiator PIA shall:

a) negate the I/O signal so that this can be distinguished from reselection;

b) assert its assigned SCSI ID, assert the requested SCSI ID of the target, negate all other DATA BUS signals and generte valid parity;

c) if an attention flag is set, assert the ATN signal;

d) release the BSY signal after two deskew delays have elapsed.

10.3.2 Selection indication

The selection indication contains the selection IDs, the attention flag, and the parity flag.

When the SEL signal and the SCSI ID bit assigned to the target PIA are true and the BSY and I/O signals are false for at least a bus settle delay the target PIA shall:

a) examine the DATA BUS for valid parity;

b) if valid parity is not detected, set the parity flag;

c) if valid parity is detected, clear the parity flag;

d) if the ATN signal is true, set the attention flag;

e) if the ATN signal is false, clear the attention flag;

f) set the selection IDs to the contents of the DATA BUS;

g) generate a selection indication.

Valid parity is determined by the rules in table 11.

Table 11 — Parity checking rules

Check for odd parity on:	If at least one bit is active on:
DB(7-0),P	DB(31-0,P,P1,P2,P3)
DB(15-8),P1	DB(31-8,P1,P2,P3)
DB(23-16),P2	DB(31-16,P2,P3)
DB(31-24),P3	DB(31-16,P2,P3)

NOTE - These rules are necessary to permit inter-operation of devices with different DATA BUS widths. For example, if a 16-bit device selects a 32-bit device, the 32-bit device will observe invalid parity on the upper 16 bits of the data bus.

10.3.3 Selection response

The selection response contains a selection accepted flag.

When a selection response is received by the target PIA, the target PIA shall:

a) if the selection accepted flag is set, assert the BSY signal within a selection abort time of the time when the target last detected that the SEL signal and the SCSI ID bit assigned to the target PIA were true, and the BSY and I/O signals were false.
b) if the selection accepted flag is cleared, release the BSY signal.

10.3.4 Selection confirmation

The selection confirmation contains the arbitration lost flag, a selection won flag, and a selection time-out flag.

If the arbitration was lost (see 10.3.1), the PIA shall:

a) release the SEL signal within two deskew delays;
b) clear the selection won flag;
c) set the arbitration lost flag;
d) clear the selection time-out flag;
e) generate a selection confirmation.

If the arbitration was won, the initiator PIA shall wait at least a bus settle delay from the completion of the selection request before examining the BSY signal. When the initiator PIA detects the BSY signal is true within a selection timeout delay of the selection request, it shall:

a) release the SEL signal after two deskew delays;
b) set the selection won flag;
c) clear the arbitration lost flag;
d) clear the selection time-out flag;
e) generate a selection confirmation.

When the initiator PIA has not detected the BSY signal to be true within a selection timeout it shall continue asserting the SEL signal and shall release all DATA BUS signals. If the initiator PIA has not detected the BSY signal to be true within at least a selection abort time plus two deskew delays of releasing the DATA BUS signals, it shall:

a) release the SEL signal;
b) clear the selection won flag;
c) clear the arbitration lost flag;
d) set the selection time-out flag;
e) generate a selection confirmation.

If the initiator PIA does detect the BSY signal to be true within at least a selection abort time plus two deskew delays of releasing the DATA BUS signals as described in the previous paragraph, it shall:

a) release the SEL signal after two deskew delays;
b) set the selection won flag;
c) clear the arbitration lost flag;
d) clear the selection time-out flag;
e) generate a selection confirmation.

10.4 Reselection service

The reselection service is a confirmed service that combines arbitration with reselection. The reselection service provides a means to reconnect.

10.4.1 Reselection request

The reselection request contains the SCSI ID of the device to be reselected.

When a reselection request is received the target PIA shall arbitrate for the SCSI bus, and if successful, reselect the designated SCSI device.

To perform an arbitration the target PIA shall:

a) wait until the SEL and BSY signals are both continuously false for at least a bus settle delay;
b) not assert any SCSI BUS signal within a bus free delay of step a) above;
c) assert the BSY signal, assert its SCSI ID, and release all other DATA BUS signals no sooner than a bus free delay and no later than a bus set delay of step a)above;

Note 16 - There is no maximum delay before asserting the BSY signal and the SCSI ID following the bus free delay in step b) as long as the SEL and BSY signals remain false. However, SCSI devices that delay longer than a bus settle delay plus a bus set delay from the time when the BSY and SEL signals first become false may fail to participate in arbitration when competing with faster SCSI devices.

d) wait at least an arbitration delay (measured from the assertion of the BSY signal) and then examine the DATA BUS to determine which SCSI IDs are true.
e) If a higher priority SCSI ID exists on the DATA BUS, then arbitration has been lost. The target PIA shall release the BSY signal and its SCSI ID within a bus clear delay after the SEL signal becomes true. The PIA proceeds to reselection confirmation (see 10.4.4).
f) If a higher priority SCSI ID does not exist on the DATA BUS then arbitration has been won. The target PIA shall assert the SEL signal. It shall change any signals until at least a bus clear delay plus a bus settle delay has elapsed after asserting the SEL signal. The target PIA proceeds to reselection.

To perform a reselection the target PIA shall:

a) assert the I/O signal so that this can be distinguished from selection;
b) assert its assigned SCSI ID, assert the requested SCSI ID of the initiator, negate all remaining DATA BUS signals, and generate valid parity;
c) release the BSY signal after two deskew delays have elapsed.

10.4.2 Reselection indication

The reselection indication contains the reselection IDs and the parity flag.

When the SEL signal, the SCSI ID bit assigned to the initiator PIA, and the I/O signal are true and the BSY signal is false for at least a bus settle delay the initiator PIA shall:

a) examine the DATA BUS for valid parity;
b) if valid parity is not detected, set the parity flag;
c) if valid parity is detected, clear the parity flag;
d) set the reselection IDs to the contents of the DATA BUS;
e) generate a reselection indication.

Valid parity is determined by the rules in table 11.

10.4.3 Reselection response

The reselection response contains a reselection accepted flag.

If the reselection accepted flag is set, the initiator PIA shall

a) assert the BSY signal within a selection abort time of the time when the initiator last detected that the SEL and I/O signals and the SCSI ID bit assigned to the initiator PIA were true, and the BSY signal was false;

b) wait until it detects the SEL signal to be false and release the BSY signal;

If the reselection accepted flag is cleared, the initiator PIA shall release the BSY signal.

10.4.4 Reselection confirmation

The reselection confirmation contains the arbitration lost flag, a reselection won flag, and a reselection time-out flag.

If the arbitration was lost (see 10.4.1), the PIA shall:

a) release the SEL signal within two deskew delays;

b) clear the reselection won flag;

c) set the arbitration lost flag;

d) generate a reselection confirmation.

If the arbitration was won (see 10.4.1), the target PIA shall wait at least a bus settle delay from the completion of the reselection request before examining the BSY signal. When the target PIA detects the BSY signal to be true within a selection timeout delay of the reselection request, it shall:

a) also assert the BSY signal;

b) wait at least two deskew delays and release the SEL signal;

c) set the reselection won flag;

d) clear the arbitration lost flag;

e) clear the reselection time-out flag;

f) generate a reselection confirmation.

When the target PIA has not detected the BSY signal to be true within a selection timeout it shall continue asserting the SEL and I/O signals and shall release all DATA BUS signals. If the target PIA has not detected the BSY signal to be true within at least a selection abort time plus two deskew delays of releasing the DATA BUS signals, it shall:

a) release the SEL and I/O signals;

b) clear the reselection won flag;

c) clear the arbitration lost flag;

d) set the reselection time-out flag;

e) generate a reselection confirmation.

If the target PIA does detect the BSY signal to be true within at least a selection abort time plus two deskew delays of releasing the DATA BUS signals as described in the previous paragraph, it shall

a) also assert the BSY signal;

b) wait at least two deskew delays and release the SEL signal;

c) set the reselection won flag;

d) clear the arbitration lost flag;

e) clear the reselection time-out flag;

f) generate a reselection confirmation.

10.5 Command service

The command service is a confirmed service that provides the means to transfer a single command byte from the initiator to the target.

10.5.1 Command request

The command request contains no parameters.

When a command request is received the target PIA shall assert the C/D signal, negate the MSG and I/O signals, and begin an information transfer.

10.5.2 Command indication

The command indication contains no parameters.

When the C/D signal is true, the MSG and I/O signals are false, and an information transfer is detected the initiator PIA shall generate a command indication.

10.5.3 Command response

The command response contains the command byte and the attention flag.

When a command response is received by the initiator PIA, the initiator PIA shall:

a) place the command byte on the DATA BUS;
b) begin an information transfer ;
c) if the attention flag is set, assert the ATN signal at least two deskew delays prior to negating the ACK signal;
d) if the attention flag is cleared, negate the ATN signal at least two deskew delays prior to asserting the ACK signal;
e) complete the information transfer.

10.5.4 Command confirmation

The command confirmation contains the command byte, the attention flag and the parity flag.

When target PIA detects a completion of the information transfer it shall:

a) receive the command byte from the DATA BUS;
b) if valid parity is not detected, set the parity flag;
c) if valid parity is detected, clear the parity flag;
d) if the ATN signal is true, set the attention flag;
e) if the ATN signal is false, clear the attention flag;
f) generate a command confirmation.

10.6 Data out service

The data out service is a confirmed service that provides the means to transfer a data word from the initiator to the target.

10.6.1 Data out request

The data out request contains the data bus width, the transfer period, and the REQ/ACK offset.

When a data out request is received the target PIA shall negate the C/D, MSG, and I/O signals and begin an information transfer.

10.6.2 Data out indication

The data out indication contains no parameters.

When the C/D, MSG, and I/O signals are false, and an information transfer is detected, the initiator PIA shall create a data out indication to the ULP.

10.6.3 Data out response

The data out response contains the data word and the attention flag.

When a data out response is received by the initiator PIA, it shall:

a) place the data word on the DATA BUS;
b) begin an information transfer (see b));
c) if the attention flag is set, assert the ATN signal at least two system deskew delays prior to negating the ACK signal;

d) if the attention flag is cleared, negate the ATN signal at least two system deskew delays prior to asserting the ACK signal;
e) complete the information transfer.

10.6.4 Data out confirmation

The data out confirmation contains the data word, the attention flag and the parity flag.

When the target PIA detects a completion of the information transfer it shall:

a) receive the data word from the DATA BUS;
b) if valid parity is not detected, set the parity flag;
c) if valid parity is detected, clear the parity flag;
d) if the ATN signal is true, set the attention flag;
e) if the ATN signal is false, clear the attention flag;
f) generate a data out confirmation.

10.7 Data in service

The data in service is a confirmed service that provides the means to transfer a data word from the target to the initiator.

10.7.1 Data in request

The data in request contains the data word, the data bus width, the transfer period, and the REQ/ACK offset.

When a data in request is received the target PIA shall negate the C/D, and MSG signals, assert the I/O signal, place the data word on the DATA BUS, and begin an information transfer.

10.7.2 Data in indication

The data in indication contains data word and the parity flag.

When the C/D, and MSG signals are false, the I/O signal is true, and an information transfer is detected, the initiator PIA shall:

a) receive the data word from the DATA BUS;
b) if valid parity is not detected, set the parity flag;
c) if valid parity is detected, clear the parity flag;
d) generate a data in indication.

10.7.3 Data in response

The data in response contains the attention flag.

When a data in response is received by the initiator PIA, it shall:

a) if the attention flag is set, assert the ATN signal at least two system deskew delays prior to negating the ACK signal;
b) if the attention flag is cleared, negate the ATN signal at least two system deskew delays prior to asserting the ACK signal;
c) complete the information transfer.

10.7.4 Data in confirmation

The data in confirmation contains the attention flag.

When target PIA detects a completion of the information transfer it shall:

a) if the ATN signal is true, set the attention flag;
b) if the ATN signal is false, clear the attention flag;
c) generate a data in confirmation.

10.8 Status service

The status service is a confirmed service that provides the means to transfer a status byte from the target to the initiator.

10.8.1 Status request

The status request contains the status byte.

When a status request is received the target PIA shall negate the MSG signals, assert the C/D and I/O signals, place the status byte on the DATA BUS, and begin an information transfer.

10.8.2 Status indication

The status indication contains status byte and the parity flag.

When the MSG signal is false, the C/D and I/O signals are true, and an information transfer is detected the initiator PIA shall:

a) receive the status byte from the DATA BUS;
b) if valid parity is not detected, set the parity flag;
c) if valid parity is detected, clear the parity flag;
d) generate a status indication.

10.8.3 Status response

The status response contains the attention flag.

When a status response is received by the initiator PIA, it shall:

a) if the attention flag is set, assert the ATN signal at least two deskew delays prior to negating the ACK signal;
b) if the attention flag is cleared, negate the ATN signal at least two deskew delays prior to asserting the ACK signal;
c) complete the information transfer.

10.8.4 Status confirmation

The status confirmation contains the attention flag.

When the target PIA detects a completion of the information transfer, it shall:

a) if the ATN signal is true, set the attention flag;
b) if the ATN signal is false, clear the attention flag;
c) generate a status confirmation.

10.9 Message out service

The message out service is a confirmed service that provides the means to transfer a single message out byte from the initiator to the target.

10.9.1 Message out request

The message out request contains no parameters.

When a message out request is received the target PIA shall assert the C/D and MSG signals, negate the I/O signal and begin an information transfer.

10.9.2 Message out indication

The message out indication contains no parameters.

When the C/D and MSG signals are true, the I/O signal are false, and an information transfer is detected, the initiator PIA shall generate a message out indication.

10.9.3 Message out response

The message out response contains the message out byte and the attention flag.

When a message out response is received by the initiator PIA, it shall:

a) place the message out byte on the DATA BUS;
b) begin an information transfer (see b));
c) if the attention flag is set, assert the ATN signal at least two deskew delays prior to negating the ACK signal;
d) if the attention flag is cleared, negate the ATN signal at least two deskew delays prior to asserting the ACK signal;
e) complete the information transfer.

10.9.4 Message out confirmation

The message out confirmation contains the message out byte, the attention flag and the parity flag.

When target PIA detects a completion of the information transfer, it shall:

a) receive the message out byte from the DATA BUS;
b) if valid parity is not detected, set the parity flag;
c) if valid parity is detected, clear the parity flag;
d) if the ATN signal is true, set the attention flag;
e) if the ATN signal is false, clear the attention flag;
f) generate a message out confirmation.

10.10 Message in service

The message in service is a confirmed service that provides the means to transfer a message in byte from the target to the initiator.

10.10.1 Message in request

The message in request contains the message in byte.

When a message in request is received the target PIA shall assert the C/D, MSG and I/O signals, place the message in byte on the DATA BUS, and begin an information transfer.

10.10.2 Message in indication

The message in indication contains message in byte and the parity flag.

When the C/D, MSG, and I/O signals are true, and an information transfer is detected, the initiator PIA shall:

a) receive the message in byte from the DATA BUS;
b) if valid parity is not detected, set the parity flag;
c) if valid parity is detected, clear the parity flag;
d) generate a message in indication.

10.10.3 Message in response

The message in response contains the attention flag.

When a message in response is received by the initiator PIA, it shall:

a) if the attention flag is set, assert the ATN signal at least two deskew delays prior to negating the ACK signal;
b) if the attention flag is cleared, negate the ATN signal at least two deskew delays prior to asserting the ACK signal;
c) complete the information transfer.

10.10.4 Message in confirmation

The message in confirmation contains the attention flag.

When the target PIA detects a completion of the information transfer, it shall:

a) if the ATN signal is true, set the attention flag;
b) if the ATN signal is false, clear the attention flag;
c) generate a message in confirmation.

10.11 Information transfer

Information transfers on the DATA BUS follow a defined REQx/ACKx transaction (RAT). The beginning of an information transfer occurs with the assertion of REQx. An information transfer is by detected by the assertion of REQx within a valid service request. The completion of an information transfer depends on the type of transfer and is defined in 10.11.1 and 10.11.2.

COMMAND, STATUS, MESSAGE OUT, and MESSAGE IN services use asynchronous RATs and transfer one byte of information with each RAT.

DATA OUT and DATA IN services use RATs and transfer a word of information with each RAT. When the data bus width is greater than 16, the REQQ and ACKQ signals are used to transfer the upper bytes of the word over the secondary SCSI bus. The REQQ and ACKQ signals are used in the same fashion as the REQ and ACK signals, but due to propagation time differences, the timing between the two sets of signals may not be identical. In the timing descriptions in this clause, references to the REQx and ACKx signals apply between the REQ and ACK signals for all RATs and between the REQQ and ACKQ signals for RATs involving data bus widths greater than 16.

The RAT may be either asynchronous or synchronous depending on the value REQ/ACK offset. A REQ/ACK offset of zero specifies an asynchronous RAT; any non-zero value specifies a synchronous RAT.

The information transfer services use a RAT to control the information transfer. Each RAT allows the transfer of one word of information.

The target PIA shall continuously assert BSY from the time of response to selection or confirmation of reselection until a bus free request is received or a reset indication occurs.

The target PIA shall continuously maintain the state of the phase signals (see Table 12) until a request is received that causes a change of state for any phase signal. The phase signals shall be valid for a bus settle

Table 12 — Information transfer services

Phase signal			Service request	Direction of transfer
MSG	C/D	I/O		
0	0	0	DATA OUT	Initiator to target or initiator role port to target-role port
0	0	1	DATA IN	Initiator from target
0	1	0	COMMAND	Initiator to target
0	1	1	STATUS	Initiator from target
1	0	0	*	
1	0	1	*	
1	1	0	MESSAGE OUT	Initiator to target
1	1	1	MESSAGE IN	Initiator from target
Key: 0 = False, 1 = True, * = Reserved for future standardization				

delay before the first information transfer and remain valid until a request is received that causes a change in the phase signals.

All non-OR-tied signals not specifically stated to be asserted shall be negated. All OR-tied signals not specifically stated to be asserted shall be released.

If a service request is different from the previous service request (i.e., the new request results in a change to one or more of the C/D, I/O, or MSG signals) then the following restrictions apply:

a) When switching the DATA BUS direction from out (initiator PIA driving) to in (target PIA driving), the target PIA shall delay driving the DATA BUS by at least a data release delay plus a bus settle delay after asserting the I/O signal and the initiator PIA shall release the DATA BUS no later than a data release delay after the transition of the I/O signal to true.

b) When switching the DATA BUS direction from in (target PIA driving) to out (initiator PIA driving), the target PIA shall release the DATA BUS no later than a deskew delay after negating the I/O signal.

10.11.1 Asynchronous information transfer

The DATA IN requests and DATA OUT requests which contain a REQ/ACK offset value of zero shall transfer the word asynchronously.

The target PIA shall control the direction of information transfer by means of the I/O signal. When the I/O signal is true, information shall be transferred from the target PIA to the initiator PIA. When the I/O signal is false, information shall be transferred from the initiator PIA to the target PIA.

If the I/O signal is true (transfer to the initiator PIA), the target PIA shall first assert the DATA BUS signals to the desired value, delay at least one deskew delay plus a cable skew delay, then assert the REQx signal. The DATA BUS signals shall remain valid until the ACKx signal is true at the target PIA. The initiator PIA shall read the DATA BUS signals after the REQx signal is true, then indicate its acceptance of the data by asserting the ACKx signal. When the ACKx signal becomes true at the target PIA, the target PIA may change or release the DATA BUS signals and shall negate the REQx signal. After the REQx signal is false the initiator PIA shall then negate the ACKx signal. After the ACKx signal is false the target PIA may continue the transfer by driving the DATA BUS signals and asserting the REQx signal, as described above.

If the I/O signal is false (transfer to the target PIA) the target PIA shall request information by asserting the REQx signal. The initiator PIA shall drive the data and parity signals to their desired values, delay at least one deskew delay plus a cable skew delay and assert the ACKx signal. The initiator PIA shall continue to drive the data and parity signals until the REQx signal is false. When the ACKx signal becomes true at the target PIA, the target PIA shall read the data and parity signals then negate the REQx signal. When the REQx signal becomes false at the initiator PIA, the initiator PIA may change or release the data and parity signals and shall negate the ACKx signal. The target PIA may continue the transfer by asserting the REQx signal, as described above.

10.11.2 Synchronous data transfer

The DATA IN requests and DATA OUT requests which contain a REQ/ACK offset value greater than zero shall transfer the word synchronously. During synchronous data transfers, a REQx (or ACKx) pulse is defined as a transition of the REQx (or ACKx) signal from false to true and back to false.

The initiator PIA shall detect a REQx pulse after the transition of the REQx signal from false to true. The target PIA shall detect an ACKx pulse after the transition of the ACKx signal from false to true.

Synchronous data transfer allows the non-interlocked data transfers between the initiator PIA and target PIA after the first REQx pulse and before the REQ/ACK offset is reached. The target PIA shall generate REQx pulses independent of the ACKx pulses until the REQ/ACK offset is reached. The initiator PIA shall generate ACKx pulses independent of the REQx pulses until the number of ACKx pulses equals the number of REQx pulses detected.

The REQ/ACK offset specifies the maximum number of REQx pulses that can be sent by the target PIA in advance of the ACKx pulses received from the initiator PIA, establishing a pacing mechanism. If the number of REQx pulses exceeds the number of ACKx pulses by the REQ/ACK offset, the target PIA shall not assert the REQx signal until after the leading edge of the next ACKx pulse is received. A requirement for successful completion of the data service is that the number of ACKx and REQx pulses be equal.

The target PIA shall assert the REQx signal for a minimum of a transmit assertion period. The target PIA shall then wait at least the greater of a transfer period from the last transition of the REQx signal to true or a minimum of a transmit negation period from the last transition of the REQx signal to false before again asserting the REQx signal.

The initiator PIA shall send an ACKx pulse for each REQx pulse received. The ACKx signal may be asserted as soon as the leading edge of the corresponding REQx pulse has been received. The initiator PIA shall assert the ACKx signal for a minimum of a transmit assertion period. The initiator PIA shall wait at least the greater of a transfer period from the last transition of the ACKx signal to true or for a minimum of a transmit negation period from the last transition of the ACKx signal to false before asserting the ACKx signal.

If the I/O signal is true (transfer to the initiator PIA), the target PIA shall first set the DATA BUS to the desired value, wait at least one transmit setup time, then assert the REQx signal. The DATA BUS shall be held valid for a minimum of one transmit hold time after the assertion of the REQx signal. The target PIA shall assert the REQx signal for a minimum of an assertion period. The target PIA may then negate the REQx signal and change or release the DATA BUS. The initiator PIA shall read the value on the DATA BUS within one receive hold time of the transition of the REQx signal to true. The initiator PIA shall then respond with an ACKx pulse.

If the I/O signal is false (transfer to the target PIA), the initiator PIA shall transfer one word for each REQx pulse. After receiving the leading edge of a REQx pulse the initiator PIA shall first set the DATA BUS to the desired value, delay at least one transmit setup time, then assert the ACKx signal. The initiator PIA shall hold the DATA BUS valid for at least one transmit hold time after the assertion of the ACKx signal. The initiator PIA shall assert the ACKx signal for a minimum of a transmit assertion period. The initiator PIA may then negate the ACKx signal and may change or release the DATA BUS. The target PIA shall read the value of the DATA BUS within one receive hold time of the transition of the ACKx signal to true.

10.11.3 Data path width

The DATA IN and DATA OUT services contain a data bus width parameter that specifies the width of the data path used to transfer the word.

During 8-bit data transfers, the logical data byte for each data service shall be transferred across the DB(7-0,P) signals on the primary SCSI bus. The DB(15-8,P1) signals are undefined and parity may not be valid. Subsequent data bytes are likewise transferred using DB(7-0,P).

During 16-bit wide data transfers, the first and second logical data bytes for each data service shall be transferred across the DB(7-0,P) and DB(15-8,P1) signals, respectively, on the primary SCSI bus. Subsequent pairs of data bytes are likewise transferred in parallel across the primary SCSI bus (see Figure 12).

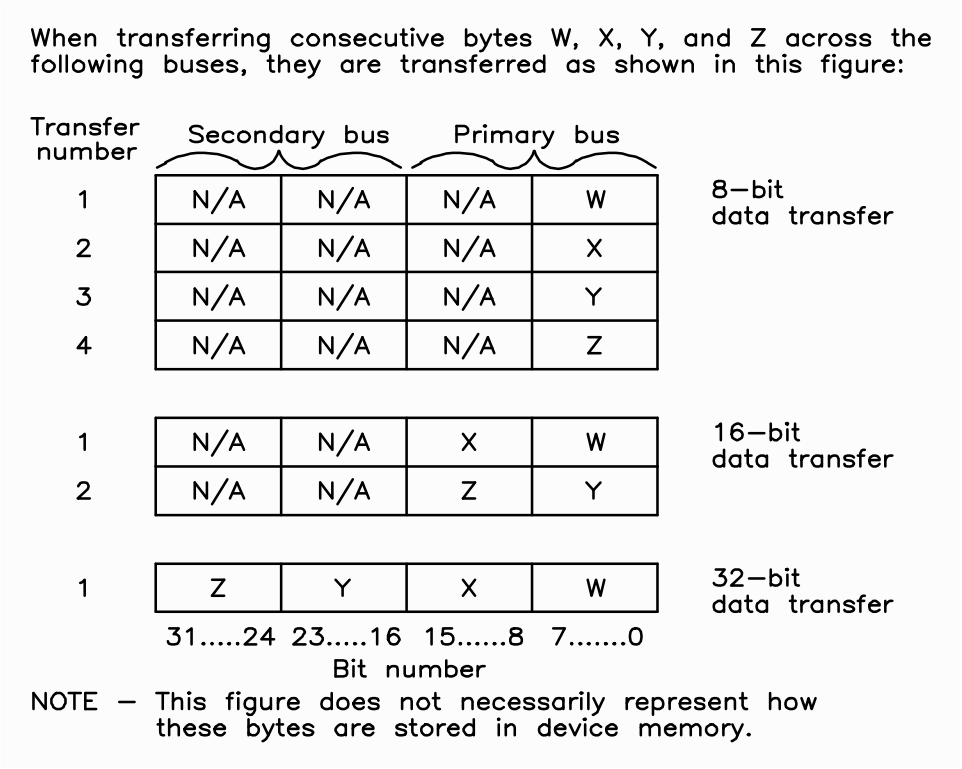


Figure 12 — Wide SCSI byte order

During 32-bit wide data transfers the first and second logical data bytes shall be transferred across the DB(7-0,P) and DB(15-8,P1) signals, respectively. The third and fourth logical data bytes shall be transferred across the DB(23-16,P2) and DB(31-24,P3) signals, respectively. Subsequent sets of four of data bytes are likewise transferred in parallel (see Figure 12).

If the last logical data byte transferred does not fall on the DB(15-8) signals for a 16-bit wide transfer or the DB(31-24) signals for a 32-bit wide transfer, then the values of the remaining higher-numbered bits are undefined. However, parity bits for these undefined bytes shall be valid for whatever data is placed on the bus.

To ensure proper data integrity on a 32-bit wide data bus, certain sequence requirements shall be met between the primary SCSI bus and the secondary SCSI bus:

a) The REQQ and ACKQ signals shall only be asserted during DATA IN and DATA OUT services. These signals shall not be asserted during other services.

b) The same information transfer mode (asynchronous or synchronous) shall be used for both the primary and secondary SCSI busses. If synchronous data transfer mode is in effect, the same REQ/ACK offset and transfer period shall be used for both busses.

c) The target PIA shall ensure that the number of RATs on both the primary and secondary SCSI busses in a data service are equal before it changes to another service. The target PIA shall not a new service (i.e.after confirmation), until the ACK and ACKQ signals have both become false for the last RAT.

If any violations of these rules are detected by the target PIA, the target PIA shall indicate a service protocol error to the ULP.

The only pacing mechanism available for a target PIA to manage the timing relationship between the signals on the two busses is its management of the REQ and REQQ signals. Similarly, the only pacing mechanism for the initiator PIA to manage the timing between the two busses is its management of the ACK and ACKQ signals.

Annex A

(normative)

Removal and insertion of SCSI devices

This annex defines the physical requirements for removal and insertion of SCSI devices on the SCSI bus. The issues related to the logical configuration of the SCSI bus and characteristics of the SCSI devices when a replacement occurs are beyond the scope of this standard.

Four cases are addressed. The cases are differentiated by the state of the SCSI bus when the removal or insertion occurs.

A.1 Case 1 - power-off during removal or insertion

a) All devices are power-off during physical reconfiguration.

A.2 Case 2 - RST signal asserted continuously during removal or insertion

a) The system shall be designed so that the SCSI device being inserted shall make its power ground and logic ground connections at least 1 ms prior to the connection of any device connector contact to the bus. The ground connections shall be maintained during and after the connection of the device to the bus.

b) The system shall be designed so that the SCSI device being removed shall maintain its power ground and logic ground prior to, during, and for at least 1 ms after the disconnection of any device connector contact from the bus.

Note 1 The translation of the 1 ms time to mechanical provisions is vendor specific.

A.3 Case 3 - Current I/O processes not allowed during insertion or removal

a) All I/O processes for all SCSI devices shall be quiesced.

b) The system shall be designed so that the SCSI device being inserted shall make its power ground and logic ground connections at least 1 ms prior to the connection of any device connector contact to the bus. The ground connections shall be maintained during and after the connection of the SCSI device to the bus.

c) The system shall be designed so that the SCSI device being removed shall maintain its power ground and logic ground prior to, during, and for at least 1 ms after the disconnection of any device connector contact from the bus.

d) The SCSI device being removed or inserted shall employ transceivers that conform to the requirements for glitch-free power on/off in 7.1.2 and 7.2.2. The SCSI device shall maintain the high-impedance state at the device connector contacts during a power cycle until the transceiver is enabled. Power cycling includes on board TERMPWR cycling, caused by plugging, and device power cycling caused by plugging and switching. Note that any on board switchable terminators as well as device transceivers may affect the impedance state at the device connector contacts.

e) The power to the electronics and mechanics of the device may be simultaneously switched with the bus contacts if the power distribution system is able to maintain adequate power stability to other devices during the transition and the grounding requirements in items b) and c) above are met.

f) The SCSI bus termination shall be external to the device being inserted or removed.

A.4 Case 4 - Current I/O process allowed during insertion or removal

a) All I/O processes for the SCSI device being inserted or removed shall be quiesced. All other SCSI devices on the bus shall have receivers that conform to the provisions in 7.1 and 7.2.

b) A device being inserted shall make its power ground and logic ground connection at least 1 ms prior to the connection of any device connector contact to the bus. The ground connections shall be maintained during and after the connection of the device to the bus.

c) A device being removed shall maintain its power ground and logic ground prior to, during, and for at least 1 ms after the disconnection of any device connector contact from the bus.

d) The SCSI device being removed or inserted shall employ transceivers that conform to the requirements for glitch-free power on/off in 7.1.2 and 7.2.2. The SCSI device shall maintain the high-impedance state at the device connector contacts during a power cycle until the transceiver is enabled.

e) The SCSI device being removed or inserted shall employ transceivers that conform to the requirements for glitch-free power on/off in 7.1.2 and 7.2.2. The SCSI device shall maintain the high-impedance state at the device connector contacts during a power cycle until the transceiver is enabled. Power cycling includes on board TERMPWR cycling, caused by plugging, and device power cycling caused by plugging and switching. Note that any on board switchable terminators as well as device transceivers may affect the impedance state at the device connector contacts.

f) The power to the electronics and mechanics of the device may be simultaneously switched with the bus contacts if the power distribution system is able to maintain adequate power stability to other devices during the transition and the grounding requirements in items b) and c) above are met.

g) The SCSI bus termination shall be external to the device being inserted or removed.

h) Bypassing capacitors connecting to the TERMPWR line on the device being inserted or removed shall not exceed 10 uF. For single ended applications, bus termination shall use voltage regulation on both ends (reference SCSI-2 alternative 2).

Annex B
(normative)
SCSI configured automatically (SCAM)

B.1 Model

The SCAM protocol is defined by this annex. SCAM is defined to ease user problems with the configuration of SCSI ID's on an SCSI bus. Level 2 SCAM defines all the hardware and software requirements necessary to implement all the functionality described in this annex. Level 1 SCAM defines a subset that requires less capable hardware and software; although it does not support all of the advanced features of level 2 (such as hot plugging) it is intended to solve most configuration problems common to the single-user system. Implementation of the SCAM protocol is optional, however, if implemented, the SCSI SCAM protocol shall conform to this annex.

B.2 Definitions

For the purposes of this annex, the following definitions apply in addition to those in the body of the standard.

assigned ID. An SCSI ID which has been inherently (in the case of SCAM tolerant devices), explicitly (by SCAM protocol) or implicitly (by SCSI selection of a minimum duration) established for an SCSI device. When an ID is assigned it also becomes the current ID. Similarly, once an ID is assigned any change to the device's current ID by non-SCAM means (e.g., a MODE SELECT command) also changes the assigned ID.

current ID. The SCSI ID that is available to an SCSI port. It may originate from jumpers, switches, mode parameters or some other source.

SCAM device. Any SCSI device, initiator or target, that implements the SCAM protocol defined in this annex.

SCAM initiator: A SCAM device that is capable of initiating SCAM selection and performing the normal functions of an SCSI initiator. These capabilities permit a SCAM initiator to scan an SCSI bus to discriminate between SCAM tolerant and SCAM devices and assign ID's to the SCAM devices.

SCAM target. A SCAM device that is capable of recognizing and responding to SCAM selection. This capability permits a SCAM target to receive an ID assignment from a SCAM initiator. A SCAM target shall have a current ID, even when it is unassigned.

SCAM tolerant. An SCSI device which does not implement the SCAM protocol but which complies with certain requirements specified by this annex. SCAM tolerant devices can be detected by a SCAM initiator and may be intermixed with SCAM devices.

unassigned ID. The current SCSI ID which is available to the device but has not yet been assigned to the device.

B.3 SCAM requirements

B.3.1 Configuration requirements

SCAM configuration requirements permit SCAM tolerant, level 1 SCAM and level 2 SCAM devices to operate on the same SCSI bus. These requirements are:

a) SCAM intolerant devices (i.e., legacy SCSI devices which are not SCAM tolerant) are not permitted on the bus;

b) Any SCSI initiator on the bus shall be a SCAM initiator;

c) No more than one level 1 SCAM initiator is permitted on the bus;

d) Multiple level 2 SCAM initiators are permitted on the bus, which they may share with up to one level 1 SCAM initiator;

e) All SCAM tolerant and level 1 SCAM targets on the bus shall be powered on before or concurrently with a SCAM initiator;

f) If the only SCAM initiator is a level 1 SCAM initiator, all devices should be powered on before or concurrently with the level 1 SCAM initiator. Level 2 SCAM targets will not be detected by the level 1 SCAM initiator until a subsequent reset condition on the bus.

Some of these configuration requirements may be overcome by means outside the scope of this annex.

B.3.2 Timing requirements

Unless otherwise indicated, the time measurements for each SCAM or SCAM tolerant device, shown in table B.1, shall be measured for signal conditions existing at that SCSI device's own SCSI bus connection.

Table B.1 — SCAM timing values

Description	Value
SCAM tolerant power-on to selection delay	5 s
SCAM tolerant reset to selection delay	250 ms
SCAM tolerant selection response time	1 ms
SCAM unassigned ID selection response delay	4 ms
SCAM power-on to SCAM selection delay	1 s
SCAM reset to SCAM selection delay	250 ms
SCAM selection response time	250 ms
Recommended SCAM selection response time	1 ms
Wide arbitration time	7.2 us

B.3.2.1 SCAM tolerant power-on to selection delay

The maximum time a SCAM tolerant device may delay after power-on before enabling its response to selection.

B.3.2.2 SCAM tolerant reset to selection delay

The maximum time a SCAM tolerant device may delay after a reset condition before enabling its response to selection.

B.3.2.3 SCAM tolerant selection response time

A SCAM tolerant device shall respond to selection of its current ID within this time limit, provided that both the SCAM tolerant power-on to selection and reset to selection delays have been satisfied.

A SCAM initiator should use a minimum selection timeout of a SCAM tolerant selection response time plus two bus settle delays when scanning the bus for SCAM tolerant devices.

B.3.2.4 SCAM unassigned ID selection response delay

The minimum time a SCAM device shall delay before responding to selection of its current ID, provided that the SCAM device has not been assigned an ID since the last power-on or reset condition.

A SCAM initiator should use a maximum selection timeout of a SCAM unassigned ID selection response delay when scanning the bus for SCAM tolerant devices.

B.3.2.5 SCAM power-on to SCAM selection delay

The minimum time a SCAM device shall delay after power-on before initiating SCAM protocol.

B.3.2.6 SCAM reset to SCAM selection delay

The minimum time a SCAM device shall delay after a reset condition before initiating SCAM protocol.

B.3.2.7 SCAM selection response time

The maximum time a SCAM device shall require to detect and respond to SCAM selection. This is also the minimum time a SCAM device should maintain SCAM selection in situations where a slow response by other SCAM devices is anticipated (e.g. firmware SCAM implementations).

B.3.2.8 Recommended SCAM selection response time

The minimum time a SCAM device should maintain SCAM selection in situations where a rapid response by other SCAM devices is anticipated (e.g. hardware SCAM implementations). This is also the recommended maximum time a SCAM device should require to detect and respond to SCAM selection.

B.3.2.9 Wide arbitration time

The maximum time after the assertion of BSY within which a SCAM device with an ID greater than 7 shall conclude its examination of the data bus to determine the outcome of arbitration.

Note 2 This requirement is necessary for arbitration without an ID to work on mixed width buses. It is based on the assumption that all wide SCSI devices implement arbitration logic in hardware and therefore can be relied on to assert the SEL signal quickly if they win arbitration.

B.3.3 Device requirements

The following subclauses define the operational requirements of SCAM and SCAM tolerant devices that may be configured on the same SCSI bus.

In addition, all SCAM devices shall disable active negation of SCSI bus signals during SCAM protocol.

B.3.3.1 SCAM tolerant target

A SCAM tolerant target:

a) shall enable its response to selection within a SCAM tolerant power-on to selection delay after the device is powered-on.

b) shall enable its response to selection within a SCAM tolerant reset to selection delay after a reset condition.

c) shall recognize a valid selection of the device's current ID whether an initiator ID is present or not during SELECTION phase.

d) shall, once selection response is enabled, recognize a valid selection of its current ID and assert the BSY signal no later than a SCAM tolerant selection response time after the start of the SELECTION phase.

The current ID becomes the assigned ID when the SCAM tolerant device responds to selection.

Note 3 It is recommended that initiators clear the DiscPriv bit in the IDENTIFY message if selection is performed without an initiator ID.

Note 4 The requirement for rapid response to selection by SCAM tolerant devices and delayed response to selection by SCAM devices that do not have assigned ID's permits SCAM initiators to distinguish between the two. A SCAM initiator may use a relatively short selection timeout (SCAM tolerant selection response time plus two bus settle delays) to scan the bus for SCAM tolerant devices without causing the assignment of an ID.

B.3.3.2 Level 1 SCAM initiator

A level 1 SCAM initiator:

a) shall recognize reset conditions at all times, regardless of whether the bus is in an SCSI phase or SCAM protocol.

b) shall be capable of initiating SCAM protocol and utilizing SCAM function sequences to assign ID's to SCAM devices. Level 1 SCAM initiators are not required to detect or respond to SCAM selection.

c) shall be capable of detecting a Dominant Initiator Contention function code and subsequently participate in the isolation stage for the dominant initiator.

Note 5 It is recommended that level 1 SCAM initiators perform Dominant Initiator Contention each time SCAM protocol is initiated.

d) shall have an assigned ID.

e) shall be able to operate with a selection timeout greater than the SCAM tolerant selection response time and less than the SCAM unassigned ID selection response delay. A level 1 SCAM initiator shall also be able to operate with a selection timeout greater than the SCAM unassigned ID selection response delay.

f) shall not assert the RST signal upon a selection timeout.

g) shall satisfy the requirements for a SCAM tolerant device.

B.3.3.3 Level 1 SCAM target

A level 1 SCAM target:

a) shall recognize reset conditions at all times, regardless of whether the bus is in an SCSI phase or SCAM protocol.

b) shall enable its response to SCAM selection within a SCAM power-on to SCAM selection delay after the device is powered-on.

c) shall enable its response to SCAM selection within a SCAM reset to SCAM selection delay after a reset condition.

d) shall, once SCAM selection response is enabled and provided that its device ID is unassigned, recognize and respond to SCAM selection within a SCAM selection response time.

e) shall recognize a valid selection of the device's current ID, provided the SELECTION phase is continuously valid for longer than a SCAM unassigned ID selection response delay. Response to selection causes the device to have an assigned ID equal to its current ID.

f) shall, once assigned an ID, behave as a SCAM tolerant device until a subsequent power-on or reset condition. Note that SCAM devices with assigned ID's neither recognize, respond to nor initiate SCAM selection.

g) shall not assert the RST signal upon a selection timeout.

h) shall implement the hard reset alternative.

B.3.3.4 Level 2 SCAM initiator

A level 2 SCAM initiator:

a) shall recognize reset conditions at all times, regardless of whether the bus is in an SCSI phase or SCAM protocol.

b) shall be capable of initiating SCAM protocol and utilizing SCAM function sequences to assign ID's to SCAM devices. Level 2 SCAM initiators are also required to detect and respond to SCAM selection initiated by other SCAM devices.

c) shall perform dominant initiator contention each time SCAM protocol is initiated.

d) shall have either an assigned ID or be able to arbitrate without an ID.

e) shall be able to operate with a selection timeout greater than the SCAM tolerant selection response time and less than the SCAM unassigned ID selection response delay. A level 2 SCAM initiator shall also be able to operate with a selection timeout greater than the SCAM unassigned ID selection response delay.

f) shall not assert the RST signal upon a selection timeout.

g) shall, provided an assigned or current ID is available, satisfy the requirements for a SCAM tolerant device.

Note 6 A level 2 SCAM initiator without a current ID may receive an assigned ID by one of two methods: either it assigns itself an ID or, by means of SCAM protocol functions, is assigned an ID by another SCAM initiator. A level 2 SCAM initiator that has a current ID may receive an assigned ID by either of these two methods or its current ID may become its assigned ID if a SELECTION phase for the current ID is continuously valid for longer than a SCAM unassigned ID selection response delay.

B.3.3.5 Level 2 SCAM target

A level 2 SCAM target:

a) shall recognize reset conditions at all times, regardless of whether the bus is in an SCSI phase or SCAM protocol.

b) shall enable its response to SCAM selection within a SCAM power-on to SCAM selection delay after the device is powered-on.

c) shall enable its response to SCAM selection within a SCAM reset to SCAM selection delay after a reset condition.

d) shall, once selection response is enabled and provided that the device ID is unassigned, recognize and respond to SCAM selection within a SCAM selection response time.

e) shall recognize a valid selection of the device's current ID, provided the SELECTION phase is continuously valid for longer than a SCAM unassigned ID selection response delay. Response to selection causes the device to have an assigned ID equal to its current ID.

f) shall, once assigned an ID, behave as a SCAM tolerant device until a subsequent power-on or reset condition. Note that SCAM devices with assigned ID's neither recognize, respond to nor initiate SCAM selection.

g) shall not assert the RST signal upon a selection timeout.

h) shall implement the hard reset alternative.

i) shall be capable of arbitration without an ID. Subsequent to power-on, a level 2 SCAM target shall initiate SCAM protocol provided that the device does not have an assigned ID and no reset condition has occurred.

B.4 SCAM protocol

SCAM is a distributed algorithm collectively executed by a group of participating SCAM devices. The communication is accomplished by shared (wired-OR) SCSI bus signals that may be asserted or released by the SCAM devices, but which shall not be negated by any participating device. Any SCAM device which is capable of active negation of SCSI bus signals shall disable active negation during SCAM protocol.

B.4.1 Initiation

A device initiates the SCAM protocol by first winning bus arbitration, then performing SCAM selection. The device may arbitrate using its current ID or it may arbitrate without an ID. After winning arbitration the device has the BSY and SEL signals asserted. It shall release all DATA BUS signals and assert the MSG signal, then wait at least two deskew delays and release the BSY signal. It shall maintain this pattern of the SEL and MSG signals asserted with the BSY signal released for a minimum of a recommended SCAM selection response time, then release the MSG signal. After releasing the MSG signal the device shall wait, using wired-OR glitch filtering (see table B.1), until the MSG signal has been released by all other devices.

Level 2 SCAM initiators and SCAM targets that have not yet been assigned an ID recognize SCAM selection if a pattern of the SEL and MSG true and the BSY signal false is detected. After a variable delay, devices responding to SCAM selection release the MSG signal, then wait, using wired-OR glitch filtering, until the

MSG signal has been released by all devices. SCAM targets should release the MSG signal quickly, perhaps never asserting it at all. SCAM initiators should wait a SCAM selection response time before releasing the MSG signal.

After wired-OR glitch filtering is used to detect the MSG signal false, each SCAM device asserts the BSY signal, waits at least two deskew delays, then asserts several other signals. SCAM initiators assert the BSY signal followed by the I/O, C/D, DB(6) and DB(7) signals. SCAM targets assert the BSY signal followed by the I/O, DB(6) and DB(7) signals. After asserting its signals each device waits at least two more deskew delays, then releases the SEL signal and waits, using wired-OR glitch filtering, until the SEL signal has been released by all devices.

After detecting that the SEL signal has been released by all devices, SCAM devices release the DB(6) signal and examine the bus signals. If the C/D signal is false, then there are no SCAM initiators participating and SCAM targets shall release all signals. If the C/D signal is true, each SCAM device waits, using wired-OR glitch filtering, for the DB(6) signal to be released by all devices and then asserts the SEL signal. Initiation of the SCAM protocol is complete after the SEL signal has been asserted.

B.4.1.1 Transfer cycles

The SCAM protocol functions through sequences of transfer cycles. During each transfer cycle certain devices broadcast data to all participating SCAM devices. The actual data received is the logical-OR of the data broadcast by all the sending devices. Each transfer cycle is fully interlocked in the same sense that asynchronous data transfers are interlocked. Completion of each step of the transfer is explicitly acknowledged, and the transfer rate adapts automatically to the speed of the SCAM devices involved.

Transfer cycles use the DB(7-5) signals as handshake lines and the DB(4-0) signals as data lines. At the beginning and end of each transfer cycle the DB(7) signal is asserted while the DB(6) and DB(5) signals are released. As shown in figure B.1each device repeats the following steps for each transfer cycle:

1) Assert data on the DB(4-0) signals, if the device is broadcasting data. Devices that have no data to broadcast release these signals. All devices assert the DB(5) signal.
2) All devices release the DB(7) signal.
3) Wait, using wired-OR glitch filtering, until the DB(7) signal is released by all devices.
4) Read and latch data from the DB(4-0) signals. All devices assert the DB(6) signal.
5) All devices release the DB(5) signal.
6) Wait, using wired-OR glitch filtering, until the DB(5) signal is released by all devices.
7) Release or change the DB(4-0) signals. All devices assert the DB(7) signal.
8) All devices release the DB(6) signal.
9) Wait, using wired-OR glitch filtering, until the DB(6) signal is released by all devices.

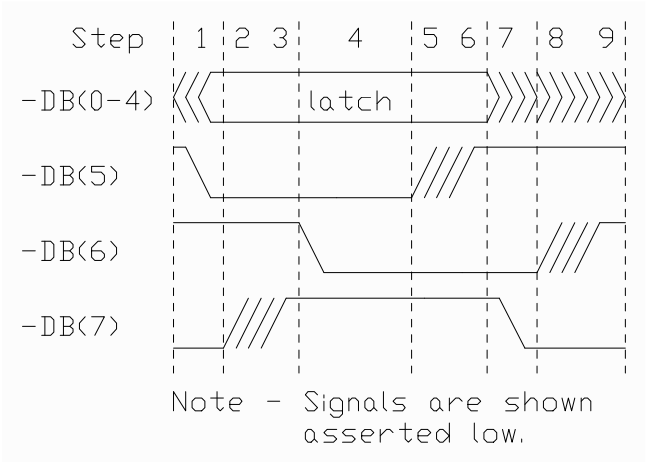


Figure B.5— Transfer cycles

The SCAM protocol continues through successive transfer cycles until the dominant SCAM initiator chooses to terminate it by releasing the C/D signal and all other signals. SCAM targets shall note the release of the C/D signal and release all signals.

B.5.1.1 Wired-OR glitch filtering

Many of the SCSI signals used by SCAM protocol are asserted by more than one SCAM device. Consequently, when one of these signals is released by a SCAM device there may be a transient period in which the signal is observed to be false even though it is still asserted by other SCAM devices. In order to eliminate these incorrect observations (and the consequent malfunction of the SCAM protocol), all SCAM devices shall perform wired-OR glitch filtering on the shared SCSI signals.

Wired-OR glitch filters may be designed into the hardware. In this case the hardware must be capable of detecting that a signal has remained continuously false for at least a bus settle delay. Note that this continuous observation of a signal requires dedicated hardware; it cannot be performed by software alone.

As an alternative, SCAM devices may implement wired-OR glitch filtering in software if the procedure described below is used. The algorithm used relies on the fact that a single device that releases a wired-OR signal can cause the signal to be incorrectly observed false for a maximum of a bus settle delay.

1) Determine the iteration count to be used in the software polling loop. This is typically 8, 16 or 32 if the SCAM device has knowledge (by means beyond the scope of this annex) that the SCSI bus can support the maximum number of devices. SCAM devices that have no means to determine the width of the SCSI bus should use an iteration count of 32.
2) If the signal is observed to be true, reset the iteration count to the initial value determined above. If the signal is observed to be false, decrement the iteration count. If the iteration count is zero, the signal has been released by all devices.
3) Wait sufficient time to guarantee that at least a bus settle delay elapses. Continue with the preceding step.

As an alternative to waiting at least a bus settle delay between samples, the implementor may wish to calculate the iteration count as follows. If the minimum sample interval is known, calculate N equal to a bus settle delay divided by the minimum sample interval. Round the number obtained up to the next higher integer. If the iteration count is set to N times the maximum number of devices on the SCSI bus, the algorithm above can be used without the need to wait between successive samples.

B.5.1.2 Isolation stage

Many SCAM function sequences require an isolation stage, which is used to isolate or identify an individual device to perform some action. During an isolation stage each participating device sends an identification string bit serially. As it sends its identification string, each participating device compares its own identification string with the strings of other devices. If a device observes a numerically higher string than its own identification string, it defers for the remainder of the function sequence and participates in subsequent function sequences only after a synchronization pattern is observed. After the isolation stage completes, only the device with the numerically highest identification string is still participating, and that device performs whatever action is specified by the function code (or subsequent action code). Identification strings are sent starting with the most significant bit of the most significant byte and ending with the least significant bit of the least significant byte.

During each transfer cycle of an isolation stage, the devices that are still participating assert the DB(0) signal if the next bit of their identification string is zero, the DB(1) signal if the next bit of their identification string is one, or release the DB(4-0) signals if they have reached the end of their identification string. SCAM initiators may assert the DB(4) signal to terminate the isolation stage prematurely. Each participating device reads the data transferred during each transfer cycle and acts on the conditions defined in table B.2.

Table B.2 — Transfer cycle conditions

Bit value	Asserted on DB(4-0)	Latched from DB(4-0)	Condition
0	00001b	00001b	Continue
		00011b	Defer
1	00010b	0001xb	Continue
none	00000b	000x1b	Defer
		0001xb	Defer
		00000b	Terminate
any	000xxb	100xxb	Terminate
		any other value	Error

The continue condition means the device shall continue to participate in the isolation stage.

The defer condition means that the device has lost to a device with a higher identification string. The device shall continue to handshake data on the DB(7-5) signals at the same time the DB(4-0) signals are released. The device shall continue in this fashion until the next synchronization pattern is observed, after which the device may respond to the function code that follows.

The terminate condition means that the isolation stage has terminated. The action to be performed by the remaining device(s) is either implicit in the function code or specified by subsequent transfer cycles in the function sequence. Usually only one SCAM device will still be participating and perform the action. However, if a SCAM initiator terminates the isolation phase by asserting the DB(4) signal, multiple devices may perform the action. SCAM targets shall not differentiate these cases, they shall act the same regardless of how the isolation stage was terminated. It is the responsibility of the SCAM initiator(s) to determine whether multiple devices remain (perhaps using configuration knowledge outside the scope of this annex) and ensure that suitable actions are performed.

The error condition implies that a bus error or reserved pattern was encountered. It is typically treated the same as the defer condition; the exact treatment is described in the individual function sequence descriptions.

SCAM initiators typically examine the identification strings for use in determining the nature of the isolated device and what action should be performed. The identification string of the isolated device is obtained from the DB(1) signal. The end of the identification string is recognized when both the DB(0) and DB(1) signals are false.

The structure of the identification string is shown in table B.3.

Table B.3 — Identification string

Bit / Byte	7	6	5	4	3	2	1	0
0	(MSB)			Type code				
1								(LSB)
2	(MSB)			Vendor identification				
9								(LSB)
10	(MSB)			Vendor specific code (up to 21 bytes)				
30								(LSB)

The identification string, at present, has a maximum length of 31 bytes. SCAM initiators shall accept identification strings up to 32 bytes total length in order to permit future SCAM protocol extensions.

The first (most significant) two bytes of a device identification string contain a type code. The contents of the type code bytes are defined in table B.4. Reserved bits in the type code shall be broadcast as zeros. A SCAM device that receives a one in any reserved bit shall defer for the remainder of the function sequence.

Table B.4 — Type code

Bit / Byte	7	6	5	4	3	2	1	0
0	Priority code		Maximum ID code		Reserved	ID Valid		SNA
1	Reserved			ID				

The priority code field contains a value specific to the function code that preceded isolation. If the function code is Isolate or Isolate and Set Priority Flag, the priority code is the device's priority flag followed by a zero. All SCAM devices maintain a priority flag, which is set to one upon power-on or after a reset condition. The value of the priority flag may also be explicitly controlled by SCAM function and action codes. If the function code is Dominant Initiator Contention, the priority code is the dominance preference code (see table B.5).

The maximum ID code encodes the largest SCSI ID that may be assigned to the device is shown in table B.5.

Table B.5 — Maximum ID code

0b	the device may be assigned an SCSI ID up to 1Fh
01b	the device may be assigned an SCSI ID up to 0Fh
10b	the device may be assigned an SCSI ID up to 07h
11b	reserved

The ID valid field encodes the validity and meaning of the contents of the ID field as defined in table B.6.

Table B.6 — ID field meaning

00b	the ID field is not valid and shall be zero
01b	the ID field contains the device's current ID but the device has not yet been assigned an ID
10b	the ID field contains the devices assigned ID
11b	reserved

All SCAM targets have a current ID, but do not necessarily have an assigned ID. It is possible for SCAM initiators to have no ID, in which case they report that the ID field is not valid.

A serial number available (SNA) bit of zero indicates the entire identification string is unavailable and will not be available until a lengthy delay (e.g., for a mechanical device access). A serial number available bit of one indicates the device's entire identification string is present. SCAM devices shall insure that both type code bytes and the most significant bit of the vendor ID code are available at all times. If the device's identification string is not yet available and the device continues to participate in the isolation stage, the device shall stall some subsequent data transfer cycle until its identification information is available.

Note 7 Some SCAM initiators may assert the DB(4) signal to terminate the isolation stage if this bit is zero, with the intention to retry the function sequence after a delay. For this reason devices should obtain their full identification string as soon as possible in preparation for future isolation stages.

The ID field contains the device's current but unassigned ID, the device's assigned ID or an undefined value as indicated by the ID valid field.

The vendor identification field contains eight bytes of ASCII data identifying the vendor of the SCAM device. The data shall be identical to the vendor identification field returned in INQUIRY data for the device.

The vendor specific code contains up to 21 bytes of data that, together with the vendor identification field, uniquely identify the SCAM device on the bus. The device vendor shall select the vendor specific code such that no two devices from the same vendor on the same bus have identical values. The recommended method for creation of the vendor specific code is to concatenate the model identification with the device serial number.

Note 8 The vendor specific code should be an ASCII data field that contains only graphic codes (i.e., code values 20h through 7Eh, inclusive). Unused bytes should occupy the least significant bytes of the field and be filled with space characters (20h).

B.5.1.3 Function sequences

Related transfer cycles are grouped into function sequences. Each function sequence serves a distinct purpose, such as assigning an ID to a single device.

Each function starts with a transfer cycle in which a synchronization pattern, all ones on the DB(4-0) signals, is broadcast. SCAM initiators assert the synchronization pattern to begin a new function sequence. SCAM targets shall recognize the synchronization pattern and begin a new function sequence regardless of whether the previous function sequence has been completed. Note that SCAM initiators may assert the synchronization pattern at any time to abort a function sequence and begin a new one.

The second transfer cycle in each function sequence specifies a function code. SCAM initiators may each assert a function code, and the resultant function code is the logical-OR of all of these codes. The operation of the function sequence and the number of subsequent transfer cycles (if any) that comprise the function sequence are determined by this resultant function code.

SCAM targets shall ignore any function sequences whose resultant function codes are reserved or are codes they do not recognize. A SCAM target ignores a function sequence by continuing the transfer cycle handshake sequence, releasing the DB(4-0) signals and ignoring the data received. This continues until the SCAM target receives the next function sequence synchronization pattern.

The following function codes are defined in table B.7.

Table B.7 — Function codes

Function Code	Description
00000b	Isolate
00001b	Isolate and set priority flag
00010b	reserved
00011b	Configuration process complete
00100b to 01110b	reserved
01111b	Dominant initiator contention
10000b to 11110b	reserved
11111b	Synchronization

B.5.1.3.1 Isolate function

This function code may be used by SCAM initiators to assign ID's to SCAM devices. After the function code, SCAM targets with unassigned ID's participate in an isolation stage. This stage normally terminates with a single SCAM target isolated. At this point, the SCAM initiator may broadcast an action code to assign an ID to the device or perform an additional function.

Note that if the SCAM initiator terminates the isolation stage by asserting the DB(4) signal more than one SCAM target may still be participating in the isolation. In this case, all the participating devices receive the action code and perform the requested operation.

Action codes are two quintets broadcast by SCAM transfer cycles on the DB(4-0) signals. In each quintet, the DB(2-0) signals contain a three-bit code value and the DB(4-3) signals contain two check bits. The value in the DB(4-3) signals is the count of zero bits present in the DB(2-0) signals. This scheme ensures conflict detection if multiple SCAM initiators erroneously broadcast different action codes.

The action codes are defined in table B.8 below.

Table B.8 — Action codes

First quintet	Second quintet	Description
11000b	ccnnnb	Assign ID 00nnnb
10001b	ccnnnb	Assign ID 01nnnb
10010b	ccnnnb	Assign ID 10nnnb
01011b	ccnnnb	Assign ID 11nnnb
10100b	11000b	Clear priority flag
	10010b	Locate on
	01011b	Locate off
	others	Reserved
others		Reserved

An action code is valid if the check bits are correct and both quintets are received. ID assignment action codes shall also specify an ID that the device can support. Isolated device(s) perform a valid action code when it is received. Transfer cycles after a valid action code and preceding the next synchronization pattern shall be ignored.

The Clear Priority Flag action code instructs the isolated device(s) to clear the priority flag. This function is typically used when the SCAM initiator wishes to defer the assignment of an ID to the isolated device(s) until a later function sequence.

The Locate On and Off action codes instruct the isolated device(s) to provide assistance for users or service personnel to physically locate the device. Upon receiving a Locate On action code, the recommended action is for the isolated device(s) to flash their fault indicator or activate some similar indication. The indication should be cleared upon receiving a Locate Off action code, a reset condition, after a time delay or upon other vendor specific actions or conditions.

A SCAM target that receives a valid ID assignment should release all bus signals and cease participating in the SCAM protocol until the next reset condition or power-on. SCAM targets shall continue participating in the SCAM protocol if they receive any other action code, receive an invalid or reserved action code, or do not receive an action code. Failure to receive an action code is typically caused by a SCAM initiator choosing to abort a function by asserting the synchronization pattern.

B.5.1.3.2 Isolate and set priority flag function

The Isolate and Set Priority Flag function operates exactly as the Isolate function described above except that the only valid action codes are those that assign an ID to the isolated device(s). This function also causes the device's priority flag to be set to one.

B.5.1.3.3 Configuration process complete function

The Configuration Process Complete function is issued by the dominant SCAM initiator when the bus configuration is complete and no further ID's are to be assigned. SCAM initiators that did not win dominance should avoid using the bus until this function code is observed. A SCAM target with an unassigned ID that observes this function code should not respond to selection until a reset condition, power on or the assignment of an ID during a subsequent SCAM protocol invocation.

B.5.1.3.4 Dominant initiator contention function

The Dominant Initiator Contention function selects one SCAM initiator, called the dominant SCAM initiator, from possibly multiple SCAM initiators. Level 2 SCAM initiators shall perform Dominant Initiator Contention as the first function sequence following each SCAM protocol invocation. Level 1 SCAM initiators shall be capable of detecting and participating in dominant initiator contention. Level 1 SCAM initiators should also perform dominant initiator contention unless they can guarantee through non-SCAM means that they are the only initiator present. SCAM targets shall ignore dominant initiator contention.

Following a Dominant Initiator Contention function code, SCAM initiators participate in an isolation stage. After the isolation stage completes the single remaining SCAM initiator is the dominant SCAM initiator. It remains the dominant SCAM initiator until the next invocation of the SCAM protocol.

SCAM initiators shall not prematurely terminate isolation after a Dominant Initiator Contention function code. If a SCAM initiator detects the DB(4) signal true or detects an error condition during the isolation stage, it may attempt recovery by releasing all signals and waiting for BUS FREE phase, or by generating a reset condition.

Each SCAM initiator broadcasts a dominance preference code in the priority code filed of the type code bytes during isolation. The dominance preference code indicating the status of the participating SCAM initiators is defined in table B.9.

Table B.9 — Dominance preference code

00b	A level 1 SCAM initiator
01b	A level 2 SCAM initiator for which code 11b does not apply
10b	reserved
11b	A level 2 SCAM initiator that knows it was dominant in the previous invocation of the SCAM protocol or has non-SCAM knowledge that it should attempt to become the dominant SCAM initiator

B.6 SCAM operations

SCAM operations encompass all those functions, for both SCAM initiators and targets, that are necessary to differentiate SCAM tolerant and SCAM devices and to subsequently assign ID's to SCAM devices. It is necessary to understand the operations of both SCAM initiators and targets, as described below, and their interactions to obtain a clear picture of SCAM operations.

B.6.1 SCAM initiator

Subsequent to power-on, a SCAM initiator should complete its local initialization and shall wait at least a SCAM power-on to SCAM selection delay before initiating any SCSI bus activity. A SCAM initiator that is a level 1 SCAM device or that can determine by means beyond the scope of this annex that it is the dominant SCAM initiator should generate a reset condition after power-on. A level 2 SCAM initiator that cannot a priori determine that it is the dominant SCAM initiator should not generate a reset condition but should initiate SCAM protocol, as described below, as if it had detected a reset condition.

After a SCAM initiator has generated or detected a reset condition, it shall initiate SCAM protocol. The first function sequence should be a Dominant Initiator Contention function. If the SCAM initiator broadcasts the numerically highest identification string during the isolation stage, it becomes the dominant SCAM initiator. If the SCAM initiator does not have the highest identification string, it becomes a subordinate SCAM initiator.

> Note 9 Level 1 SCAM initiators are not required to perform dominant initiator contention, but they shall detect a dominant initiator contention function broadcast by another SCAM initiator. The identification string of a level 1 SCAM initiator is defined so that it cannot win contention with a level 2 SCAM initiator; thus the losing level 1 SCAM initiator assumes the role of a subordinate SCAM initiator.

Level 2 SCAM initiators shall always be enabled to detect the initiation of SCAM protocol by another level 2 SCAM device, either an initiator or a target.

B.6.1.1 Dominant SCAM initiator

A dominant SCAM initiator is responsible to categorize possible SCSI ID's as assigned or unassigned and then to assign ID's to SCAM devices as necessary. Once this process of ID assignment is complete, the dominant SCAM initiator should broadcast a Configuration Process Complete function. This function sequence has two purposes; it communicates to subordinate SCAM initiators that they may resume normal SCSI operations (and scan the SCSI bus) and it confirms that SCAM targets with unassigned ID's shall remain in this state and not respond to normal SCSI selection.

Dominant SCAM initiators may be implemented in several ways so long as the functions of SCSI ID categorization and assignment are performed as specified below.

B.6.1.1.1 SCSI ID categorization

After a reset condition, a dominant SCAM initiator shall wait as necessary to insure that a SCAM tolerant reset to selection delay has elapsed. The dominant SCAM initiator shall initialize an internal table of SCSI ID's to indicate that all SCSI ID's are uncategorized. A dominant SCAM initiator shall categorize each uncategorized ID by winning arbitration and selecting the uncategorized ID with a selection timeout delay greater than the SCAM tolerant selection response time and less than the SCAM unassigned ID selection response delay. If the dominant SCAM initiator has an assigned ID, it may use it to arbitrate, otherwise it shall arbitrate without an ID.

If a selection timeout is detected, the dominant SCAM initiator shall categorize the ID as unassigned. If the SCSI device responds to selection by asserting the BSY signal, the dominant SCAM initiator shall categorize the ID as assigned. In this case, the dominant SCAM initiator should complete an INQUIRY or similar command sequence to gracefully conclude selection of the SCSI device.

The dominant SCAM initiator shall repeat this process until all SCSI ID's have been categorized as either assigned or unassigned. Note that SCSI ID's may be categorized by means outside the scope of this annex, for example, by configuration parameters. This may eliminate the need for SCSI ID categorization altogether.

B.6.1.1.2 SCSI ID assignment

Once all SCSI ID's are categorized, the dominant SCAM initiator should initiate SCAM protocol and iteratively isolate and assign ID's to all SCAM devices. The dominant SCAM initiator should perform a Dominant Initiator Contention function sequence to guaranty that it remains the dominant initiator. If the formerly dominant SCAM initiator loses dominant initiator contention, it should continue to participate in SCAM protocol but function as a subordinate SCAM initiator.

Once the assignment of SCSI ID's is completed, through one or more instances of SCAM protocol, the dominant SCAM initiator should broadcast a Configuration Process Complete function sequence and terminate SCAM protocol.

B.6.1.2 Subordinate SCAM initiator

A subordinate SCAM initiator shall continue to participate in the SCAM protocol and respond to all SCAM function sequences. If the subordinate SCAM initiator does not have an assigned ID, this is necessary so that the dominant SCAM initiator may assign an SCSI ID. Unlike a SCAM target, a subordinate SCAM initiator should not release all signals and stop participation in SCAM protocol once it has been assigned an ID. Instead, it should recognize only synchronization patterns and the Configuration Process Complete function sequence.

If the subordinate SCAM initiator detects the termination of SCAM protocol but has not observed a Configuration Process Complete function sequence, it shall not resume normal SCSI operations. Level 2 SCAM initiators shall continue to be able to detect the initiation of SCAM protocol.

B.6.2 Level 1 SCAM target

Level 1 SCAM target operation is illustrated in figure B.2 below. State names are referenced in the description that follows. Note a reset condition shall cause an exit from any state and places the SCAM target in the Reset Delay state.

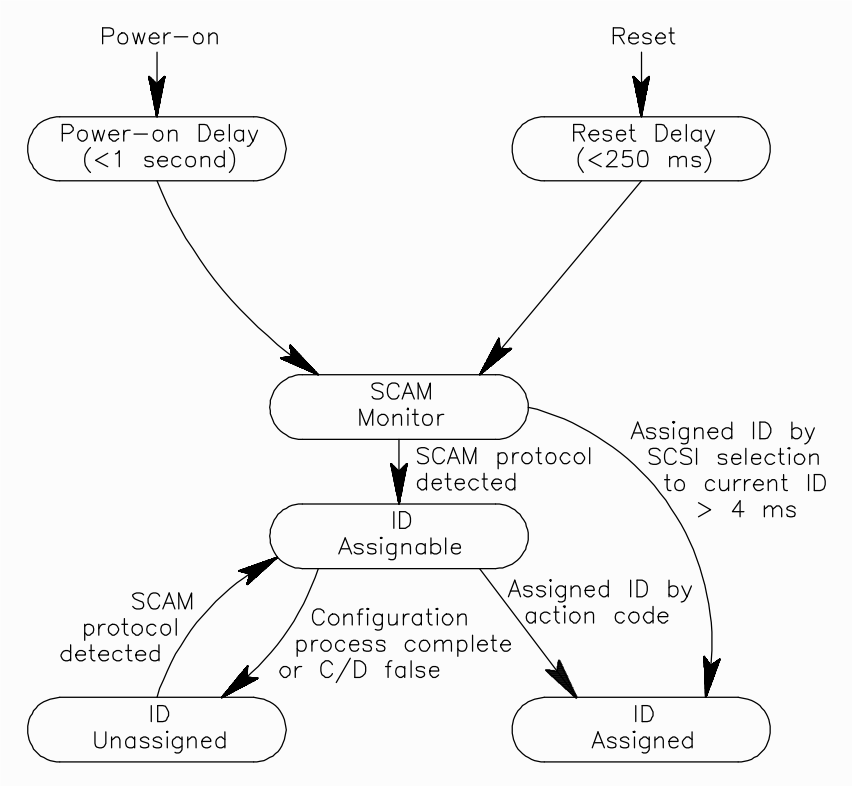


Figure B.7— Level 1 SCAM target states

When a SCAM target is powered-on, it immediately enters the Power-On Delay state and may perform local initialization. The SCAM target shall leave this state and enter the SCAM Monitor state within a SCAM power-on to SCAM selection delay.

While in the SCAM Monitor state, a SCAM target shall monitor the SCSI bus for both SCAM selection and normal SCSI selection. If the SCAM target detects the initiation of SCAM protocol, it shall enter the ID Assignable state. If a SELECTION phase for the SCAM target's current ID is continuously valid for at least a SCAM unassigned ID selection response delay, the SCAM target shall respond to selection and assert the BSY signal. This response to selection implicitly causes the SCAM target to enter the ID Assigned state just as if an explicit ID assignment had been received. The assigned ID is set to the current ID and the SCAM target now functions as a SCAM tolerant device.

A SCAM target remains in the ID Assignable state as long as SCAM protocol is maintained until explicit SCAM functions change its state. If a SCAM target is isolated and receives an Assign ID action code, the ID specified becomes both the current and assigned ID. The SCAM target releases all SCSI bus signals and enters the Assigned ID state. If the SCAM target receives a Configuration Process Complete function code or if SCAM protocol is terminated (the C/D signal is false), it should release all SCSI bus signals and enter the ID Unassigned state.

> Note 10 Some SCAM targets do not recognize the Configuration Process Complete function code and return to the SCAM Monitor state when SCAM protocol is terminated.

A SCAM target in the ID Unassigned state has not had any SCSI ID explicitly or implicitly assigned and shall not respond to SCSI selections for its current ID regardless of the duration. With the exception of a power-on or reset condition, only the detection of SCAM protocol initiation shall cause the SCAM target to leave the ID Unassigned state.

Once a SCAM target has reached the ID Assigned state it functions as a SCAM tolerant device with the ID assigned. That is, it shall respond to SCSI selection within a SCAM tolerant selection response time and shall not recognize nor respond to SCAM selection.

A reset condition shall cause a SCAM target to enter the Reset Delay state, in which it may perform local initialization. The SCAM target shall leave this state and enter the SCAM monitor state within a SCAM reset to SCAM selection time.

B.7.3 Level 2 SCAM target

Level 2 SCAM target operation is illustrated in Figure B-3 below. State names are referenced in the description that follows. Note a reset condition shall cause an exit from any state and places the SCAM target in the Reset Delay state.

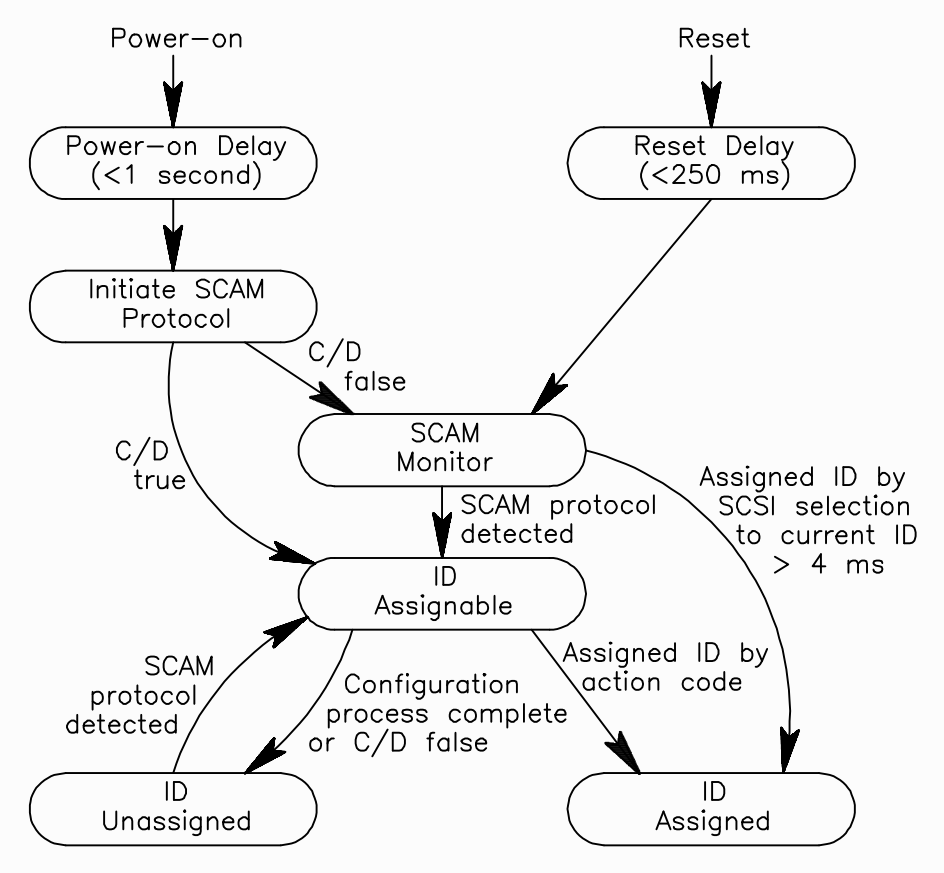


Figure B.8— Level 2 SCAM target states

When a SCAM target is powered-on, it immediately enters the Power-On Delay state and may perform local initialization. The SCAM target shall leave this state and enter the Initiate SCAM Protocol state within a SCAM power-on to SCAM selection delay.

In the Initiate SCAM Protocol state, a level 2 SCAM target shall arbitrate for the SCSI bus without an ID and perform SCAM selection. After a SCAM selection delay, the SCAM target shall examine the SCSI bus to determine the state of the C/D signal. If the C/D signal is true, there is a SCAM initiator present and the SCAM target shall enter the ID Assignable state. If the C/D signal is false, no SCAM initiator is present and the SCAM target shall enter the SCAM Monitor state. Note that level 2 SCAM targets make only one attempt to initiate SCAM protocol after power-on.

While in the SCAM Monitor state, a SCAM target shall monitor the SCSI bus for both SCAM selection and normal SCSI selection. If the SCAM target detects the initiation of SCAM protocol, it shall enter the ID Assignable state. If a SELECTION phase for the SCAM target's current ID is continuously valid for at least a

SCAM unassigned ID selection response delay, the SCAM target shall respond to selection and assert the BSY signal. This response to selection implicitly causes the SCAM target to enter the ID Assigned state just as if an explicit ID assignment had been received. The assigned ID is set to the current ID and the SCAM target now functions as a SCAM tolerant device.

A SCAM target remains in the ID Assignable state as long as SCAM protocol is maintained until explicit SCAM functions change its state. If a SCAM target is isolated and receives an Assign ID action code, the ID specified becomes both the current and assigned ID. The SCAM target releases all SCSI bus signals and enters the Assigned ID state. If the SCAM target receives a Configuration Process Complete function code or if SCAM protocol is terminated (the C/D signal is false), it should release all SCSI bus signals and enter the ID Unassigned state.

> Note 11 Some early implementations of SCAM targets do not recognize the Configuration Process Complete function code and return to the SCAM Monitor state when SCAM protocol is terminated.

A SCAM target in the ID Unassigned state has not had any SCSI ID explicitly or implicitly assigned and shall not respond to SCSI selections for its current ID regardless of the duration. With the exception of a power-on or reset condition, only the detection of SCAM protocol initiation shall cause the SCAM target to leave the ID Unassigned state.

Once a SCAM target has reached the ID Assigned state it functions as a SCAM tolerant device with the ID assigned. That is, it shall respond to SCSI selection within a SCAM tolerant selection response time and shall not recognize nor respond to SCAM selection.

A reset condition shall cause a SCAM target to enter the Reset Delay state, in which it may perform local initialization. The SCAM target shall leave this state and enter the SCAM monitor state within a SCAM reset to SCAM selection time.

Annex C

(informative)

Interconnecting buses of different widths

A problem may occur when mixing SCSI-3 devices with SCSI-1 or SCSI-2 devices. The TERMPWR requirements (see table 7) of SCSI-3 have been increased to support a 16-bit data bus. SCSI-1 and SCSI-2 devices may not supply sufficient TERMPWR. An additional source of TERMPWR (e.g., an SCSI-3 device) may be required.

When busses of dissimilar width are adapted to one another as shown in figures C.1 and C.2, the DATA BUS signals from the wider of the two busses that end at the adapter should be terminated at the adapter. The connectors are designed such that A and P shielded connectors will not intermate directly.

Two of the RESERVED lines (A cable contact numbers 23 and 24) and the OPEN line (A cable contact number 25) on the A cable are TERMPWR lines on the P cable (P cable contact numbers 33, 34, and 35).

8-bit devices that are connected to the single-ended P cable should leave the following 9 signals open:DB(8-15),DB(P1).

8-bit devices that are connected to the differential P cable should leave the following 18 signals open: +DB(15-8),-DB(15-8), +DB(P1),-DB(P1).

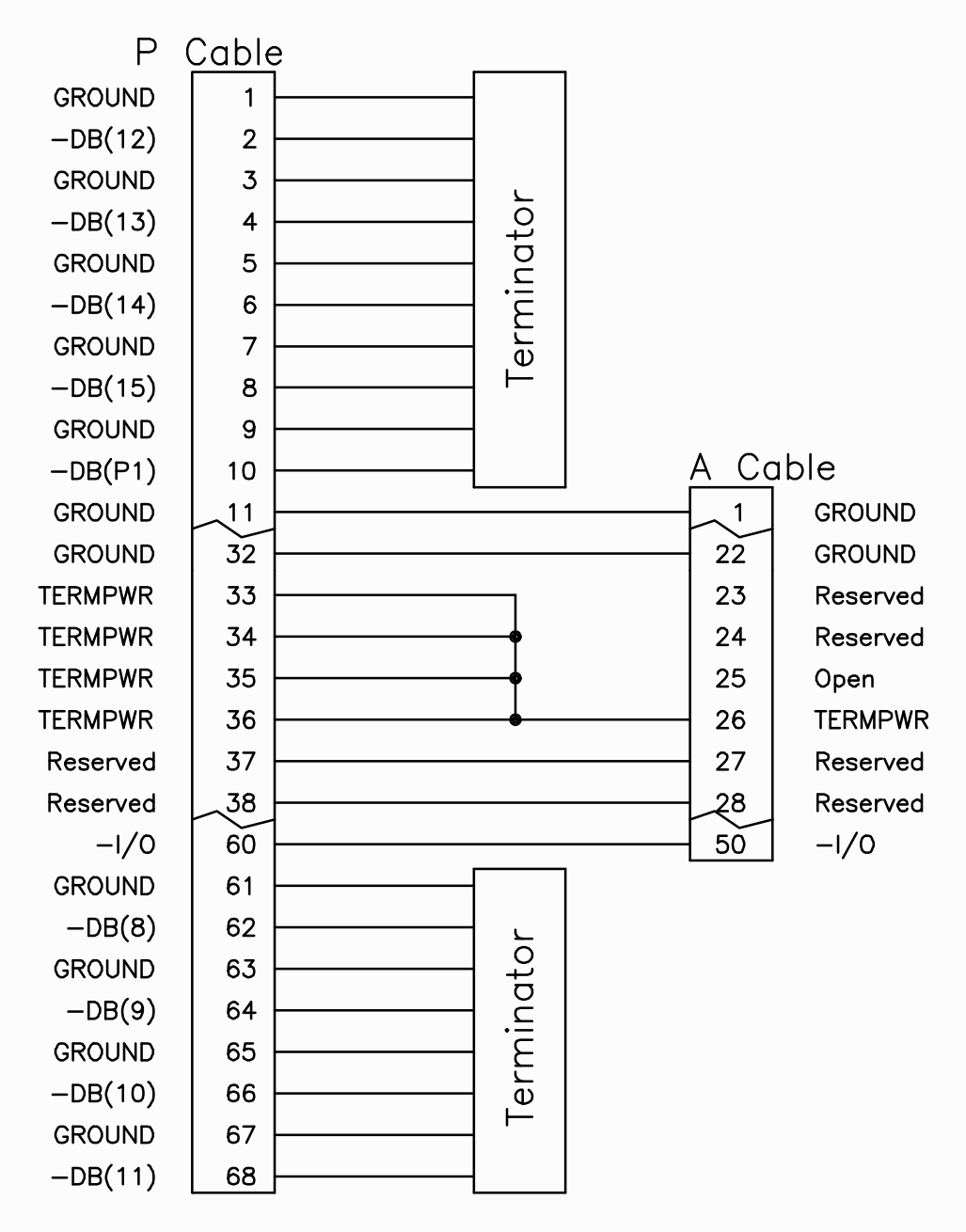


Figure C.1 — Interconnecting single-ended A and P cables

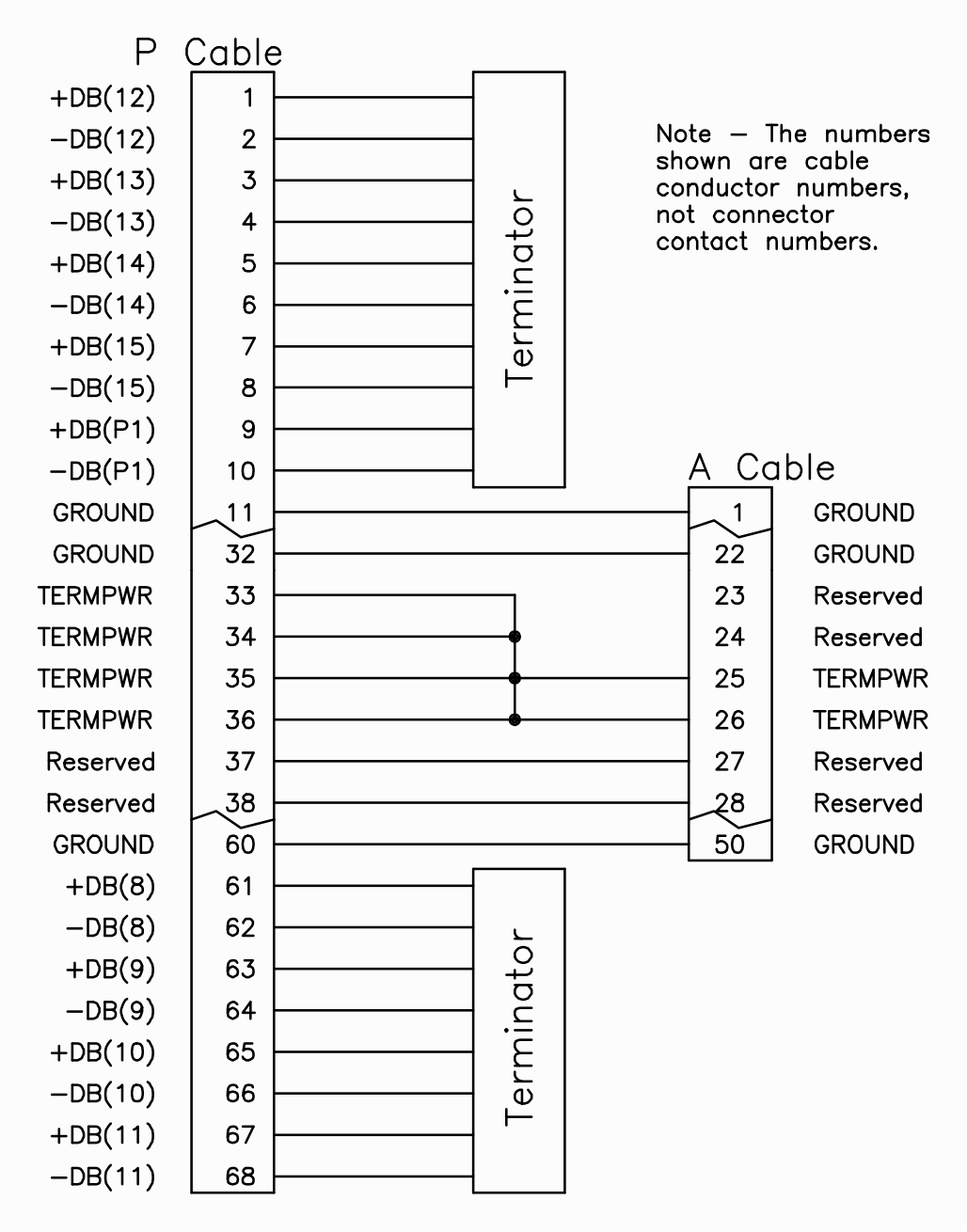


Figure C.2− Interconecting differential A and P cables

Annex D

(informative)

Cabling and cable measurement method recommendations

D.1 Cabling

To minimize discontinuities and signal reflections, the use of cables with different impedances in the same bus should be minimized. Implementations may require trade-offs in shielding effectiveness, cable length, the number of loads, transfer rates, and cost to achieve satisfactory system operation. To minimize discontinuities due to local impedance variation, a flat cable should be spaced at least 1,27 mm (0,050 in) from other cables, any other conductor, or the cable itself when the cable is folded. Also, use of 26 AWG wire in 1,27 mm (0,050 in) pitch flat cable will more closely match impedances of many round shielded cables, resulting in fewer impedance discontinuities and therefore, improved signal quality.

When mixing devices of different widths, particular care should be taken to not exceed the skew allowances provided by the cable skew delay and the deskew delay. These timing parameters can be lowered by reducing SCSI device input capacitance, SCSI device stub length, and the number of SCSI devices attached to the bus. The same precautions should be taken on busses with single-ended devices using fast synchronous data transfers in order to maintain system integrity.

D.2 Cable measurement

The following test procedures are recommended for measuring cable parameters. In addition to the referenced standards, single-ended measurements are made between the signal wire of the pair under test and the ground wire of all pairs connected to the shield.

The following procedure prepares the cable sample for the testing of differential impedance, single-end mode impedance and propagation delay.

a) Cut sample cable length to 6 m.

b) Remove 50 cm of outer jacket at each end of the cable sample.

c) Comb out braid wire strands to form a pigtail.

d) Trim filler and tape materials.

e) Strip insulation from all conductors at both cable ends 6 cm.

D.2.1 Impedance, TDR, single-ended

Using a time domain reflectometer with a 500 ps maximum rise time, on a 6 m cable sample length, measure the cable impedance between the signal wire of a particular pair and the ground wire of all pairs connected to the shield. The impedance will be averaged between 2 ns and 4 ns from the test fixture/cable interface.

D.2.2 Impedance, TDR, differential

On a 6 m (20 ft) cable sample length, select the pair to be measured. Tie all other wires and the shield together. Using a time domain reflectometer with a 500 ps maximum rise time, make the three measurements indicted in figure D.1. The values for each measurement are to be averaged between 2 ns and 4 ns from the test fixture/cable interface.

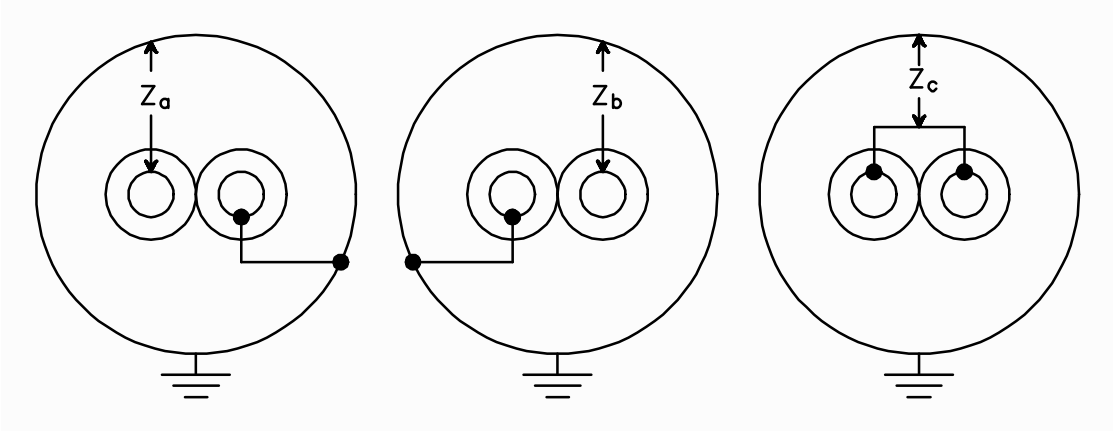


Figure D.1— Differential impedance measurement

Calculate the differential impedance of the cable using the following equation:

$$\frac{4Z_c(Z_z + Z_b)}{8Z_c - (Z_a + Z_b)}$$

Differential impedance measurements may also be performed using single and dual step differential time domain reflectometers.

D.1.3 Attenuation, differential

Measured in accordance with ASTM D-4566 at a test frequency of 5 Mhz.

D.1.4 Velocity (propagation delay) and skew

Propagation delay is the time it takes a signal to traverse a length of cable. Using a pulse generator with a 1 ns maximum rise time and an oscilloscope or a time domain reflectometer, on a 6 m (20 ft), cable sample length, select the pair to be evaluated. The shield and other pairs are unterminated. Measure the difference between the input and output signal corresponding to the 50% level.

Propagation delay skew is the difference between the maximum and minimum measured propagation delay.

D.1.5 D.C. resistance

Measured in accordance with ASTM D-4566.

Annex E

(informative)

Setup and hold timing

Figures E.1 and E.2 show how the setup and hold times are calculated for various physical configurations. SCSI timing is specified at the SCSI connectors. To calculate the setup and hold timings for SCSI protocol chips, the following examples are provided.

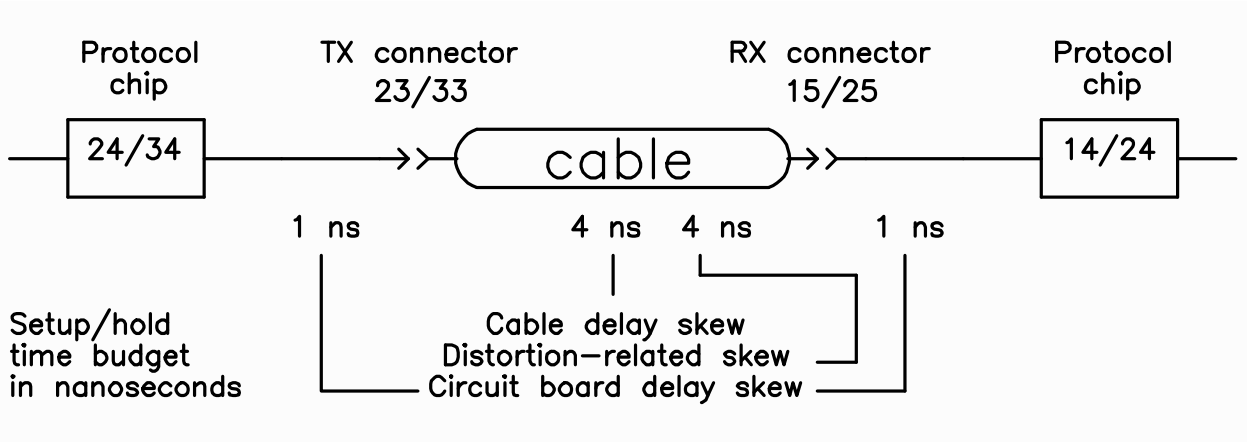


Figure E.1— Setup and hold times for single-ended applications

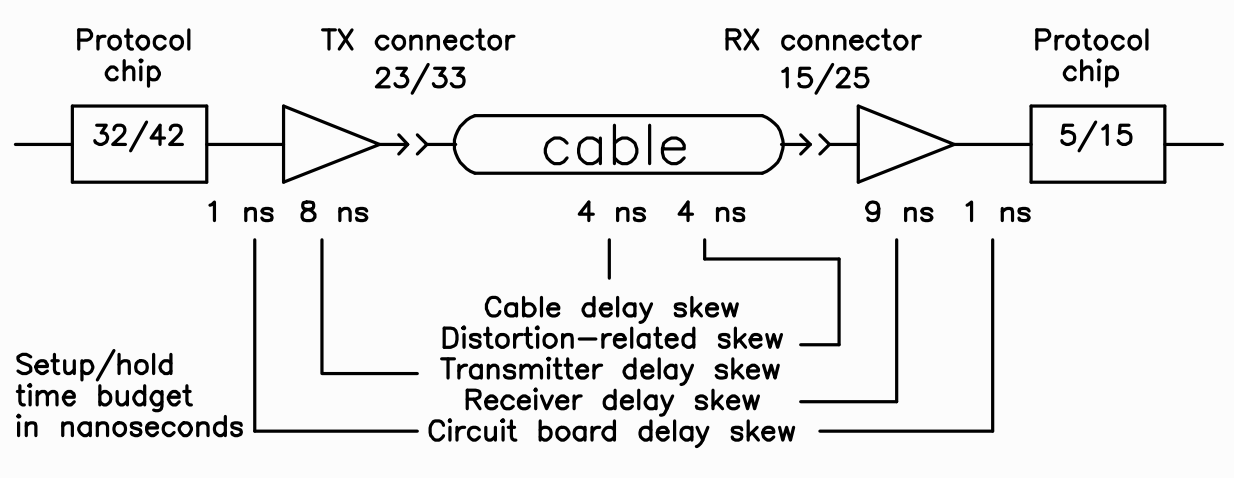
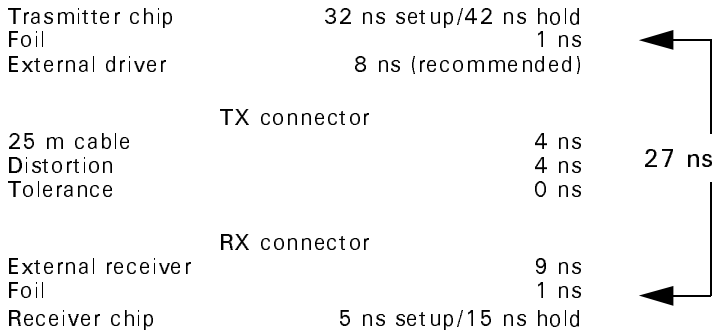


Figure E.2— Setup and hold timing for differential applications

The receiver delay skew is the maximum difference in propagation delay time between any two receivers on the REQ, REQQ, ACK, ACKQ, DATA BUS or parity signals of the same bus when external receivers are used.

The transmitter delay skew is the maximum difference in propagation delay time between any two transmitters on the REQ, REQQ, ACK, ACKQ, DATA BUS or parity signals of the same bus when external transmitters are used.

In systems with external transceivers, the total skew budget is 27 ns.



At its connector, the transmitting SCSI device should

a) drive data no less than 23 ns before asserting the REQx or ACKx signal;

b) keep that data valid for no less than 33 ns following the assertion of the REQx or ACKx signal.

The receiving device shall be able to latch the data at its connector when

a) data is valid no more than 15 ns prior to the false-to-true transition of the REQx or ACKx signal;

b) data is valid no more than 25 ns following the false-to-true transition of REQx or ACKx signal.

When 9 ns is added to the transmit device timing for transmitter skew and skew due to foil delays, the transmitting SCSI chip setup and hold timings are 32 ns and 42 ns, respectively. Similarly, when 10 ns is subtracted from the skew budget of the receiving device, 5 ns and 15 ns are left for receive chip setup and hold, respectively.

In the case of fast timing with no external transceivers over a 25 m cable, the total skew budget is 10 ns, compared to 27 ns. The 17 ns difference is used to relax the timing at the SCSI protocol chips (8 ns for the transmitting chip, and 9 ns for the receiving chip).

Note 12: Component vendors may require that differential drivers and receivers be operated within restricted voltage and temperature differences to achieve the specified transmitter and receiver delay skew values.

Annex F

(informative)

Terminator, impedance, crosstalk, and bus length considerations

SCSI terminators serve two basic functions: to establish the voltage of passively negated lines, and to establish the currents in asserted lines. In some cases they can also be used to match line impedances to eliminate reflections.

F.1 Single-ended alternative

For SCSI signal transfers to achieve high reliability, SCSI signals at the using receivers must show monotonic transitions from above 2,0 V d.c. to below 0,8 V d.c., or vice versa, with transition times in the 5 ns to 10 ns range. For SCSI bus signals to maintain these standards when encountering lumped capacitances and stubs, it is helpful for the characteristic impedance z_0 of the bus conductors to be relatively low. But for signals to be able to achieve acceptable initial levels when released in passive negation, it is helpful for z_0 to be relatively high. The higher the assertion current furnished by the terminators, the lower the acceptable level of z_0. With the full 24 mA allowed, the minimum allowed z_0 of 72 ohm is generally satisfactory. But note that the allowed 72 ohm applies to the lowest impedance conductor used, not to the average for all the conductors in the cable.

The first widely used terminator comprised 220 ohm /330 ohm resistor pairs, SCSI-2 Alternative 1. This terminator will meet the 2,5 V minimum voltage requirement with any TERMPWR voltage of 5,0 V d.c. or more but has two important shortcomings:

a) Because it has no regulation, its effect on bus signals varies with any variations in TERMPWR voltage.

b) Even with a nominal 4,7 V d.c. of TERMPWR voltage, it provides only about 20 mA into an asserted line held at 0,2 V. Because of these shortcomings, the use of this terminator is deprecated. The Alternative 2 terminator of SCSI-2--a regulated 2,85 V d.c. circuit node linked to each line through 110 ohm resistors--does not suffer such shortcomings.

Additional margin in the passively negated signal is initially achieved if one of the two devices in a data exchange is at or is very near an end of the bus. In this case, the terminator at this end can be directly effective in improving the initial passive negation levels. Its effectiveness is enhanced if the current it sources at all signal levels is increased over what can be achieved with a simple linear circuit, such as either of those presented above--i.e., if the terminator displays a somewhat current-sourcing characteristic.

Greater margin yet in the passively negated signal is achieved by terminators that deliberately exceed the allowed 24 mA limit on current sourced into an asserted line. Although there must be a reduction in driver MTBF with this practice, experience indicates that it generally is very slight. Such extra current provides protection against lower than optimal cable impedances and possible other deficiencies in implementation. It can, however, hurt the assertion edges of signals received at the ends of long buses.

Crosstalk noise in the bus is not a problem with flat ribbon cable and is best controlled by conductor placement (clocks in the center, data around the periphery) in round, twisted-pair cables. Any other correctives may be harmful by increasing signal skew.

The 3 m and 6 m length limits suggested for 10 megatransfers per second and 5 megatransfers per second transfers, respectively, are aimed at promoting successful implementations. Where circumstances present a need for longer bus operation, special emphasis must be paid to the guidelines suggested above and in the standard:

a) limit lumped capacitance,

b) limit stub length and crowding,

c) control cable impedance,

d) control current sourced into asserted lines,

e) control crosstalk effects,

f) provide input glitch rejection in receivers,

g) place initiator PIAs at or very near bus ends, and/or,

h) use active-negation drivers on clock and data lines.

F.2 Differential alternative

The extra cost, power, and space requirements of differential implementations are compensated for by superior reliability margin. This arises from the noise rejection properties of differential signals, the approximately 1 V noise margins provided, and the fact that all differential drivers to date have provided active negation. Because of this, there has developed no demand for improvements in the original differential terminator, as presented in figure 9. However the requirement for good high-frequency bypass right at the terminator is the same as in single-ended.

Crosstalk effects can be significant in long flat ribbon cables, and for this reason the use of twisted pairs in ribbon cables is encouraged. In round twisted-pair cables, crosstalk has generally not been a significant problem.

The ratio of impedances in a cable measured in single-ended and differential modes corresponds well to the ratio of impedances set forth in this standard for the two modes of operation. Because of this, and because of the relative immunity to crosstalk, round twisted-pair cables optimized for single-ended applications are suitable for differential applications also. There is generally no need to create two separate sets of cables.

Annex G

(informative)

Measuring pin capacitance

The objective of this procedure is to determine the lumped capacitance imposed on each signal conductor of the bus proper by an SCSI device connected thereto. The model for this procedure assumes the bus in ribbon cable form passing through an insulation-displacement SCSI connector, the mating part that is mounted on an SCSI device controller printed-wire board. The bus connector is removed from the device, along with every source of power.

One or more device connector circuit-common pins are connected together to form an effective circuit-common node. An R-F admittance bridge (or equivalent), operation at 1,0 MHz, is connected successively to each signal pin in the device connector, with reference to the circuit-common node.

The signal applied during measurement shall be biased to 0,5 V d.c. and shall be 0,4 V peak-to-peak in amplitude.

The characteristics shall be determined in terms of a parallel combination of a conductance and a capacitive susceptance. The corresponding capacitance thus determined is the maximum signal capacitance referred to in 7.1.4.

Note 13: SCSI signals contain a wide range of frequency components, so that it is not practical to "tune" a bus conductor by loading it with shunt inductance. Consequently, this procedure must be performed without any inductive element connected.

Note 14: If it were desired to perform this procedure on a differential SCSI device a differential bridge must be used and this procedure modified accordingly.

Annex H

(informative)

SCSI icons

These icons are provided as symbols to identify an SCSI port and to indicate whether the port is using differential or single-ended transceivers. The icons illustrated in figures H.1 and H.2 may be enlarged or reduced as needed for the application. The text and graphic may be used together or separately. The text font and size may also be adjusted as required.

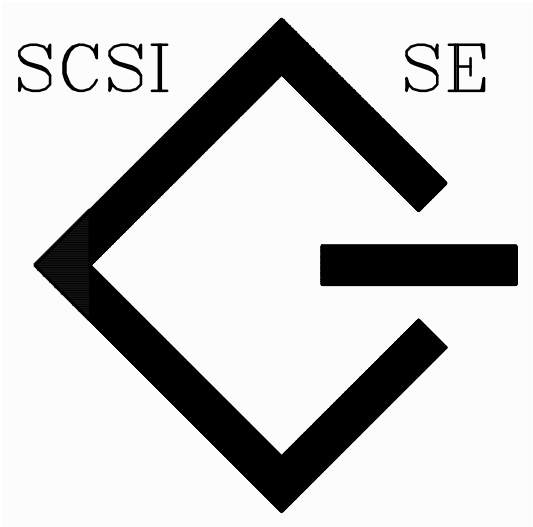


Figure H.1— Single-ended icon

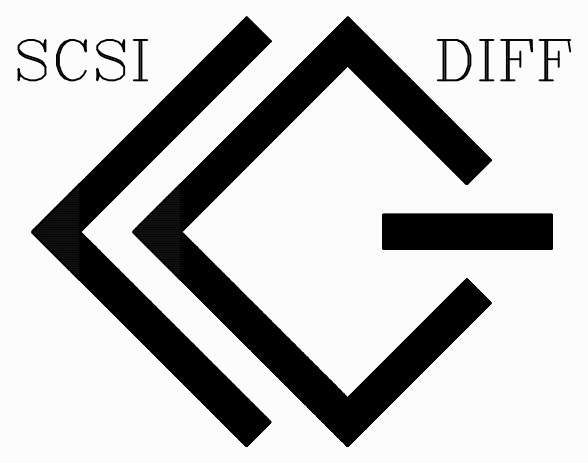


Figure H.2— Differential icon

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