International Technology Roadmap for Semiconductors

2000 Update

Overall Roadmap Technology Characteristics

TABLE OF CONTENTS

OVERALL ROADMAP TECHNOLOGY CHARACTERISTICS & GLOSSARY

BACKGROUND

The Overall Roadmap Technology Characteristics (ORTC) 2000 Update Tables have been revised from the *International Technology Roadmap for Semiconductors, 1999 edition* (ITRS) ORTC to highlight the current rapid pace of advancement in semiconductor technology. They represent a "snapshot" of the work in progress by the International Roadmap Committee (IRC) and the International Technology Working Groups (ITWGs) as they prepare for the full revision of the ITRS in 2001.

The ORTC tables are used throughout the update and renewal of the ITRS to identify rapidly changing, leading-edge trends and provide synchronization among the ITWGs. In July 2000, the IRC reached consensus on proposing "most aggressive" values for a few high-level ORTC line items that were then used to drive the complete ORTC update. These values represent the most optimistic of three scenarios (see details below) that are still under discussion in preparation for the 2001 edition of the ITRS. Thus, they represent a start toward creating new ORTC tables early in the 2001 ITRS revisondevelopment process.

With respect to the ITWG tables, the activities for the 2000 Update are limited to review and correction as possible considering all tables from the 1999 ITRS. Some ITWG tables do not comprehend this "most aggressive" ORTC 2000 Update. Inconsistencies among the ITWG and ORTC tables are part of this work-in-progress as we move towards the full revision of the ITRS in 2001. Therefore we encourage review of the ITWG tables as a response-to-date.

The 2001 activities focus on a complete revision of the ITRS. Once we have consensus on the 2001 ORTC tables, they will serve as a guide for the activities of the International Technology Working Groups in producing their detailed chapters for the 2001 edition.

The complete 1999 ITRS, along with the latest 2000 Update Tables are available for viewing and printing as an electronic document at the International SEMATECH internet web site http://public.itrs.net.

UPDATE OVERVIEW AND OBSERVATION SUMMARY

Please note that the year header on the tables may refer to different points in the development/life cycle of integrated circuits (ICs), depending on the individual line item metric. However, unless otherwise specified for a particular line item, the default year header still refers (as in previous Roadmaps) to the year when product shipment first exceeds 10,000 units per month of ICs from a manufacturing site using "production tooling." Additional clarification was provided this year by the IRC, requiring a second company to start production within 3 months. To satisfy this definition, ASIC production may represent the cumulative volume of many individual product line items processed through the facility.

Furthermore, new IRC guidelines clarified the definition of a Technology Node as the achievement of significant advancement in the process technology. To be explicit, a Technology Node was defined as the achievement of an approximate 0.7x reduction per node (0.5x per two nodes). The period of time in which a new Technology Node is reached is called a "technology-node cycle." It is acknowledged that continuous improvement occurs between Technology Nodes, and this is reflected by arithmetic interpolation between nodes in the annual columns of the "Near-Term Years" tables. The "Long Term Years" table columns are snapshots at 3-year increments and do not necessarily coincide with Technology Node Years.

In the 1998 ITRS Roadmap Update and the 1999 ITRS Renewal development, a trend was first identified which indicated that the technology node cycle had accelerated by at least one year compared to the 1997 National Technology Roadmap for Semiconductors (NTRS). Additionally, it was discussed that the technology

implementation trend could be moving from a 3-year technology-node cycle to a 2-year rate, and a pull-in of the 130nm node to 2001 was anticipated. However, by the completion of the work on the 1999 ITRS in November, 1999, the 180nm node was pulled in one year to 1999, a 3-year technology node cycle was applied, and the 130nm DRAM half-pitch node target remained in 2002.

During their 2000 ITRS Update activities, the ITWGs and the IRC have concluded that a two-year DRAM half-pitch node cycle rate will indeed be maintained through 2001, pulling in the original 1999 ITRS 130nm node target from 2002 to 2001. Beyond 2001, three possible scenarios were considered for potential technology node (DRAM half-pitch) trends, as summarized below:

Scenario 1 (Sc. 1.0): Pull-in the 130nm DRAM half-pitch to 2001, but then intersect with the original 100nm 1999 ITRS target in 2005. Next, interpolate the annual numbers in-between and extrapolate from the 100nm/2005 point at a 70%/node (0.5×/2nodes) reduction rate.

Scenario 1.5 (Sc. 1.5): Pull-in the 130nm DRAM half-pitch to 2001, but move 100nm to 2004 (a corresponding 1-year pull-in from the original 1999 ITRS point in 2005); then, interpolate the annual numbers in-between, and extrapolate from the new 100nm/2004 point at a 70%/node (0.5×/2nodes) reduction rate.

Scenario 2.0 (also known as the "Best-Case Opportunity" or "Most Aggressive" case) (Sc. 2.0): Pull-in the 130nm DRAM half-pitch to 2001, and also correct the original 100nm, 70nm, 50nm, and 35nm "nodes" to the 70%/node definition (0.5×/2nodes rate): 90nm, 65nm, 33nm, and 23nm, respectively.

Please note in Figure 1 and in Table A the 3-year node cycle is being forecast as a future trend for all scenarios. However, only the new “most aggressive” scenario proposal, Scenario 2.0, includes a correction to the IRC-defined trend rate. The new correction results in a 2-year pull-in of the sub-100-nanometer DRAM half-pitch nodes.

As previously mentioned, for simplification and focus in the 2000 Update publication, only the proposed “most aggressive” Scenario 2.0 was used to develop the complete ORTC Update Tables included in this ORTC 2000 Update document. Scenario 2.0 was also recommended by the IRC for use by the ITWGs as guidance in developing their 2000 Update Tables. The ITWGs responded in their ITWG 2000 Update tables.

For reference and ease of comparison by the reader, the original 1999 ITRS ORTC target roadmap data has been included and identified as **“1999 ITRS”** in the line item labels. The new proposal targets for the 2000 Update “most aggressive” scenario are identified as “**Sc. 2.0**” in the line item identifier, and modified targets are highlighted in **bold blue text**.

Note in Figure 1 that the “printed in resist” MPU Gate Length trend, originally introduced in the 1998/99 ITRS development, remains unchanged from its original trend, but now the leading-edge ASIC and MPU are at the same technology level. New for the 2000 Update is the addition of a trend to track the actual “Physical Bottom Gate Length” of leading-edge MPU and ASIC devices.

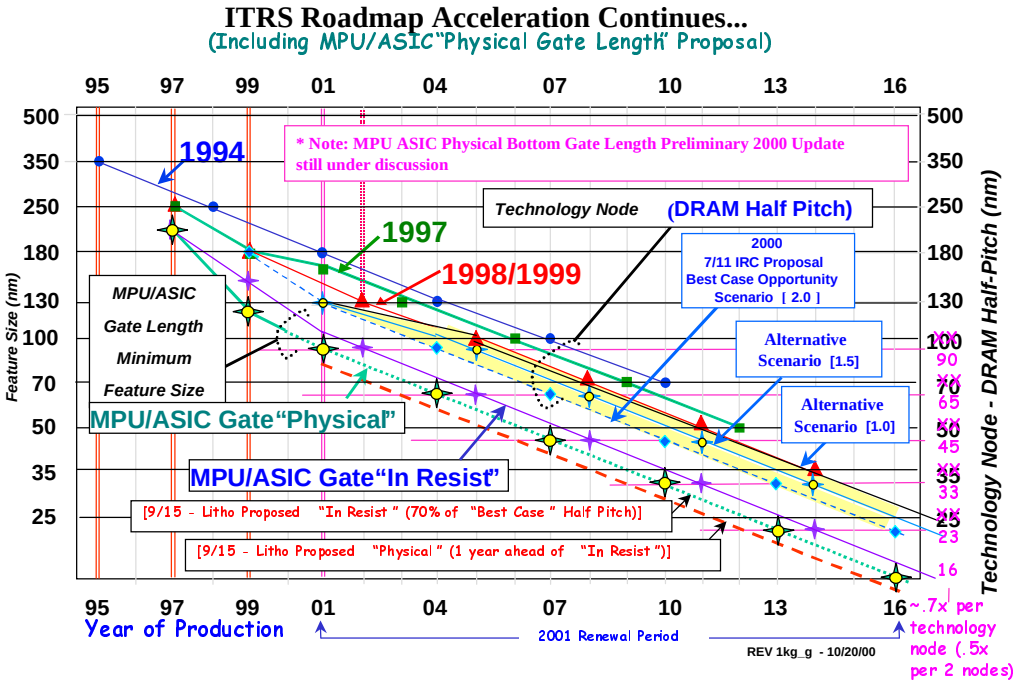

Figure 1 ITRS Roadmap Acceleration Continues...
(Including MPU/ASIC "Physical Gate Length" Proposal and Half-Pitch Trend Correction)

Table A Product Generations and Chip Size Model - ***Technology Node Scenarios***

Year of Production / *Technology Node* / ***WAS (1999 ITRS)***	*1999* *180nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*		*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
DRAM ½ Pitch (nm) ***WAS (1999 ITRS)***	180	165	150	130	120	110	100		70	50	35
DRAM ½ Pitch (nm) ***IS [Sc.1.0] [pull-in 130nm 1 year; 100nm/2005; then .7x/3yrs reduction rate]***	180	**150**	**130**	**120**	**115**	**105**	100		70	50	35
DRAM ½ Pitch (nm) ***IS [Sc. 1.5] [pull-in 130nm 1 year; 100nm/2004; then.7x/3yrs reduction rate]***	180	**150**	**130**	**120**	**110**	**100**	**90**		**65**	**45**	**33**
DRAM ½ Pitch (nm) ***IS [Sc.2.0] [pull-in 130nm 1 year; then .7x/3yrs reduction rate]***	180	**150**	**130**	**115**	**100**	**90**	**80**		**[60]§**	**[40]§**	**[30]§**

§ Note that proposed node years for Scenario 2.0 are now 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 1a Product Generations and Chip Size Model ***Technology Nodes****—Near Term Years**

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
YEAR OF PRODUCTION TECHNOLOGY NODE (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	DRIVER
Lithography-Based Characteristics								
DRAM ½ Pitch (nm) (1999)	180	165	150	130	120	110	100	D ½
DRAM ½ Pitch (nm) (SC. 2.0)	180	150	130	115	100	90	80	D ½
MPU/ASIC ½ Pitch (nm) (1999)	230	210	180	160	145	130	115	M AND A ½
MPU/ASIC ½ Pitch (nm) (SC. 2.0) [Tied to DRAM]	230	190	160	145	130	115	100	M AND A ½
MPU Gate Length (nm) †† (1999)	140	120	100	85-90	80	70	65	M GATE
ASIC Gate Length (nm) (1999)	180	165	150	130	120	110	100	A GATE
MPU/ASIC Gate Length (In Resist) (nm) †† (SC. 2.0)	140	120	100	90	80	70	65	M AND A GATE
Physical Bottom Gate-Length								
MPU/ASIC Gate Length (nm) †† [NEW]	120	100	90	80	70	65	60	COST/PERFORMANCE

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 1b Product Generations and Chip Size Model ***Technology Nodes****—Long Term Years**

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]
Lithography-Based Characteristics			
DRAM ½ Pitch (nm) (1999)	70	50	35
DRAM ½ Pitch (nm) (SC. 2.0)	60	40	30
MPU/ASIC ½ Pitch (nm) (1999)	80	55	40
MPU/ASIC ½ Pitch (nm) (SC. 2.0) [Tied to DRAM]	70	50	35
MPU Gate Length (nm) †† (1999)	45	30-32	20-22
ASIC Gate Length (nm) (1999)	70	50	35
MPU/ASIC Gate Length (In Resist) (nm) †† (SC. 2.0)	45	33	23
Physical Bottom Gate-Length			
MPU/ASIC Gate Length (nm) †† [NEW]	40	30	20

†† MPU and ASIC Gate-length (In Resist) node targets refer to most aggressive requirements, as printed in photoresist (which was by definition also "as etched in polysilicon", in the 1999 ITRS).

NEW: Trends have been identified, in which the MPU and ASIC "physical bottom" gate lengths may be reduced from the "as-printed" dimension. These "physical bottom" gate-length targets are also included in the FEP, PIDs, and Design TWG Tables as needs which drive device and process technology requirements.

* In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 1c **DRAM Production** Product Generations and Chip Size Model—Near Term Years*

YEAR OF PRODUCTION TECHNOLOGY (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
YEAR OF PRODUCTION TECHNOLOGY NODE (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	DRIVER
DRAM ½ Pitch [f] (nm) (1999)	180	165	150	130	120	110	100	D ½
DRAM ½ Pitch [f] (nm) SC. 2.0)	180	150	130	115	100	90	80	D ½
Cell area factor [A] (1999)	8.0	7.3	6.6	6.0	5.4	4.9	4.4	Market — Cost/Timing
Cell area factor [A] (SC. 2.0)	8.0	8.0	8.0	8.0	8.0	8.0	6.0	Market — Cost/Timing
Cell area [Ca = Af^2] (μm^2) (1999)	0.26	0.20	0.15	0.10	0.08	0.059	0.044	Market — Cost/Timing
Cell area [Ca = Af^2] (μm^2) (SC. 2.0)	0.26	0.18	0.13	0.10	0.082	0.065	0.039	Market — Cost/Timing
Cell array area at production (% of chip size) § (1999)	53%	—	55%	—	53%	—	54%	Market — Cost/Timing
Cell array area at production (% of chip size) § (SC. 2.0)	53.0%	54.0%	54.8%	55.3%	55.7%	56.1%	56.4%	Market — Cost/Timing
Generation at production § (1999)/(SC. 2.0)	256M	—	512M	—	1G	—	2G	Market — Cost/Timing
Functions per chip (Gbits) [NEW]	0.268	0.380	0.537	0.759	1.07	1.52	2.15	Market — Cost/Timing
Chip size at production (mm^2) § (1999)	132	—	145	—	159	—	174	Market — Cost/Timing
Chip size at production (mm^2) § (SC. 2.0)	131	129	127	141	157	175	147	Market — Cost/Timing
Gbits/cm^2 at production § (1999)	0.20	—	0.37	—	0.68	—	1.23	Market — Cost/Timing
Gbits/cm^2 at production § (SC. 2.0)	0.20	0.29	0.42	0.54	0.68	0.87	1.46	Market — Cost/Timing

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 1d **DRAM Production** Product Generations and Chip Size Model—Long Term Years*

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 [60 nm]	2011 [40 nm]	2014 [30 nm]
DRAM ½ Pitch [f] (nm) (1999)	70	50	35
DRAM ½ Pitch [f] (nm) (SC. 2.0)	60	40	30
Cell area factor [A] (1999)	3.5	3.0	2.5
Cell area factor [A] (SC. 2.0)	6.0	4.0	4.0
Cell area [Ca = Af^2] (μm^2) (1999)	0.017	0.008	0.003
Cell area [Ca = Af^2] (μm^2) (SC. 2.0)	0.019	0.0064	0.0032
Cell array area at production (% of chip size) § (1999)	52%	56%	57%
Cell array area at production (% of chip size) § (SC. 2.0)	57.3%	57.8%	58.2%
Generation at production § (1999)	[5.7]	16G	[45.2G]
Generation at production § (SC. 2.0)	[6G]	16G	[48G]
Functions per chip (Gbits) [NEW]	6.1	17.2	48.6
Chip size at production (mm^2) § (1999)	199	229	262
Chip size at production (mm^2) § (SC. 2.0)	205	191	268
Gbits/cm^2 at production § (1999)	3.05	7.51	18.5
bits/cm^2 at production § (SC. 2.0)	2.97	8.99	18.1

§ DRAM Model—**Cell Factor (design/process improvement) targets are: 1999-2004/8x; 2005-2010/6x; 2011-2016/4x. DRAM product** generations **are usually increased by** 4× bits/chip every four years with interim 2× bits/chip generations, **except: 1) at the Introduction phase, after the 8Gbit interim generation, the introduction rate is 4x/5years (2x/2-3yrs); and 2) at the Production phase, after the interim 32Gbit generation, the introduction rate is 4x/5years (2x/2-3yrs).** InTER-generation chip size growth rate **varies to maintain 1 chip per 572mm^2 field at Introduction and 2 chip per 572mm^2 field at Production. The more aggressive "best case opportunity" technology node trends allow the Production-phase products to remain at 2x bits/chip every 2 years and still fit within the target of two DRAM chips per 572mm^2 field size, through the 32Gbit interim generation.** The InTRA-generation chip size shrink model is 0.5× **every technology node in-between cell factor reductions.**

Note: Long-Term nodes now fall on: 2010/45; 2013/33; 2016/25

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 1e **DRAM Introduction** Product Generations and Chip Size Model—Near Term Years*

YEAR OF PRODUCTION TECHNOLOGY (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
YEAR OF PRODUCTION TECHNOLOGY NODE (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	DRIVER
DRAM ½ Pitch [f] (nm) (1999)	180	165	150	130	120	110	100	D ½
DRAM ½ Pitch [f] (nm) (SC. 2.0)	180	150	130	115	100	90	80	D ½
Cell area factor [A] (1999)	8.0	7.3	6.6	6.0	5.4	4.9	4.4	Market — Cost/Timing
Cell area factor [A] (SC. 2.0)	8.0	8.0	8.0	8.0	8.0	8.0	6.0	Market — Cost/Timing
Cell area [Ca = Af^2] (μm^2) (1999)	0.26	0.20	0.15	0.10	0.08	0.059	0.044	Market — Cost/Timing
Cell area [Ca = Af^2] (μm^2) (SC. 2.0)	0.259	0.183	0.130	0.103	0.082	0.065	0.039	Market — Cost/Timing
Cell array area at introduction (% of chip size) § (1999)	70%	—	72%	—	70%	—	72%	Market — Cost/Timing
Cell array area at introduction (% of chip size) § (SC. 2.0)	69.5%	70.5%	71.3%	71.8%	72.2%	72.6%	72.9%	Market — Cost/Timing
Generation at introduction § (1999)	1G	—	2G	—	4G	—	8G	—
Generation at introduction § (SC. 2.0)	1G	—	2G	—	4G	—	8G	—
Functions per chip (Gbits) (1999)	1.07	—	2.15	—	4.29	—	8.59	Market — Moore's Law
Functions per chip (Gbits) (SC. 2.0)	1.07	1.52	2.15	3.04	4.29	6.07	8.59	Market — Cost/Timing
Chip size at introduction (mm^2) § (1999)	400	—	438	—	480	—	526	Market — Cost/Timing
Chip size at introduction (mm^2) § (SC. 2.0)	400	395	390	435	485	542	454	Market — Cost/Timing
Gbits/cm^2 at introduction § (1999)	0.27	—	0.49	—	0.89	—	1.63	Market — Cost/Timing
Gbits/cm^2 at introduction § (SC. 2.0)	0.27	0.38	0.55	0.70	0.88	1.12	1.89	Market — Cost/Timing

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 1f **DRAM Introduction** *Product Generations and Chip Size Model—Long Term Years**

YEAR OF PRODUCTION TECHNOLOGY (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]
DRAM ½ Pitch [f] (nm) (1999)	70	50	35
DRAM ½ Pitch [f] (nm) (SC. 2.0)	60	40	30
Cell area factor [A] (1999)	3.5	3.0	2.5
Cell area factor [A] (SC. 2.0)	6.0	4.0	4.0
Cell area [Ca = Af²] (μm^2) (1999)	0.017	0.008	0.003
Cell area [Ca = Af²] (μm^2) (SC. 2.0)	0.019	0.0064	0.0032
Cell array area at introduction (% of chip size) § (1999)	69%	75%	75%
Cell array area at introduction% of chip size) § (SC. 2.0)	73.3%	74.3%	74.7%
Generation at introduction § (1999)	[22.6G]	64G	[181G]
Generation at introduction § (SC. 2.0)	[20G]	[45G]	[104G]
Functions per chip (Gbits) (1999)	24.3	68.7	194
Functions per chip (Gbits) (SC. 2.0)	19.7	45.3	104.2
Chip size at introduction (mm^2) § (1999)	603	691	792
Chip size at introduction (mm^2) § (SC. 2.0)	516	392	448
Gbits/cm^2 at introduction § (1999)	4.03	9.94	24.5
Gbits/cm^2 at introduction § (SC. 2.0)	3.82	11.56	23.25

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 1g ***MPU (High-volume Microprocessor) Cost-Performance*** *Product Generations and Chip Size Model—Near Term Years**

YEAR OF PRODUCTION TECHNOLOGY (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
YEAR OF PRODUCTION TECHNOLOGY NODE (Sc. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	DRIVER
Process/design annual improvement factor ++ (1999)	0.90	0.90	0.90	0.91	0.92	0.93	0.93	Market — Cost/Timing
(SC. 2.0)	1.00	1.00	1.00	0.93	0.93	0.93	0.93	
Transistor density SRAM at introduction ($Mtransistors/cm^2$) (1999)/(SC. 2.0)	35	50	70	95	128	173	234	Market — Cost/Timing
Transistor density logic at introduction ($Mtransistors/cm^2$) (1999)/(SC. 2.0)	6.6	9.4	13	18	24	33	44	Market — Cost/Timing
Generation at introduction * (1999)/(SC. 2.0)	p99c	—	p01c	—	p03c	—	p05c	—
Functions per chip (million transistors [Mtransistors]) (1999)	23.8	—	47.6	—	95.2	—	190	Market — Moore's Law
(1999)/(SC. 2.0)	23.8	33.7	47.6	67.3	95.2	135	190	
Chip size at introduction (mm^2) ‡ (1999)	340	—	340	—	372	—	408	Market — Cost/Timing
(SC. 2.0)	340	340	340	356	372	390	408	
Cost performance MPU ($Mtransistors/cm^2$ at introduction) (including on-chip SRAM) ‡ (1999)	7	—	14	—	26	—	47	M Gate and M and A ½
(SC. 2.0)	7.0	9.9	14.0	18.9	25.6	34.5	46.7	
Generation at production *	p97c	—	p99c	—	p01c	—	P03c	—
Chip size at production (mm^2) §§ (1999)	170	—	170	—	214	—	235	Market — Cost/Timing
(SC. 2.0)	170	170	170	178	186	195	204	
Cost performance MPU ($Mtransistors/cm^2$ at production, including on-chip SRAM) ‡ (1999)	7	—	14	—	22	—	41	M Gate and M and A ½
(SC. 2.0)	7.0	9.9	14.0	18.9	25.6	34.5	46.7	

++ *The MPU Process/design improvement factor is an estimate of the additional annual functional area reduction required beyond the area reduction contributed by the MPU metal half-pitch reduction. Note that this additional area reduction for transistor density plays a role generally analogous to the "cell area factor" for DRAMs. It has been achieved historically through a combination of many factors, for example: use of additional interconnect levels, self-alignment techniques, and more efficient circuit layout.*

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 1h **MPU (High-volume Microprocessor) Cost-Performance** *Product Generations and Chip Size Model—Long Term Years**

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]
Process/design improvement factor (1999)	0.93	0.93	0.93
(SC. 2.0)	0.93	0.93	0.93
Transistor density SRAM at introduction (Mtransistors/cm^2) (1999)/(SC. 2.0)	577	1,423	3,510
Transistor density logic at introduction (Mtransistors/cm^2) (1999)/(SC. 2.0)	109	269	664
Generation at introduction * (1999)/(SC. 2.0)	—	p11c	—
Functions per chip (million transistors (Mtransistors) (1999)/(SC. 2.0)	539	1,523	4,308
Chip size at introduction (mm^2) ‡ (1999)	468	536	615
(SC. 2.0)	468	536	615
Cost-performance MPU Mtransistors/cm^2 at introduction (including on-chip SRAM) ‡ (1999)	115	284	701
(SC. 2.0)	115	284	701
Generation at production * (1999)/(SC. 2.0)	—	p09c	—
Chip size at production (mm^2) § (1999)/(SC. 2.0)	269	308	354
(SC. 2.0)	**234**	**268**	**307**
Cost performance MPU Mtransistors/cm^2 at production (including on-chip SRAM) ‡ (1999)	100	247	609
(SC. 2.0)	**115**	**284**	**701**

* p is processor, numerals reflect year of introduction, c is cost-performance product.

** p is processor, numerals reflect year at ramp, h is high-performance product.

† MPU Cost-performance Model—Cost-performance MPU includes small level 1 (L1) on-chip SRAM (32Kbyte/1999), but consists primarily of logic transistor functionality; both SRAM and Logic functionality doubles every two years.

‡ MPU High-performance Model—High-performance MPU includes large level 2 (L2) on-chip SRAM (2MByte/1999) added to ramp-level cost-performance core functionality shrunk from 2-year-prior generation (P99h = 11.9M transistor (Mtransistors) (shrunk P97 core) + 98Mtransistors (2048 bytes × 8 bits/byte × 6 transistors/bit) L2 SRAM = 110Mtransistors/1999); both SRAM and Logic functionality doubles every two years.

‡ MPU High-performance Model—High-performance MPU includes large level 2 (L2) on-chip SRAM (**1**MByte/1999) added to ramp-level cost-performance core functionality shrunk from 2-year-prior generation (P99h = 11.9M transistor (Mtransistors) (shrunk P97 core) + **49**Mtransistors (1024 bytes × 8 bits/byte × 6 transistors/bit) L2 SRAM = **61**Mtransistors/1999); both SRAM and Logic functionality doubles every two years.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates **can be kept flat through 2001, due to the more aggressive MPU/ASIC half-pitch technology node trend**; but beyond 2001, the target growth rate is 1.2× growth every four years. The InTRA-generation chip size shrink model is 0.5× every two years through 2001, then 0.5× every three years after 2001.

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 1i ***High-Performance MPU and ASIC*** *Product Generations and Chip Size Model—Near Term Years**

YEAR OF PRODUCTION TECHNOLOGY (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
YEAR OF PRODUCTION TECHNOLOGY NODE (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	DRIVER
Logic (Low-volume Microprocessor) High-performance ‡								
Generation at production ** (1999)/(SC. 2.0)	p99h	—	p01h	—	p03h	—	p05h	—
Functions per chip (million transistors) (1999)	110	—	220	—	441	—	882	*Market — Moore's Law*
(SC. 2.0)	61	86	122	173	244	345	488	
Chip size at production (mm^2) § (1999)	450	—	450	—	567	—	622	*Market — Cost/Timing*
(SC. 2.0)	310	310	310	325	340	356	372	
High-performance MPU Mtransistors/cm^2 at production (including on-chip SRAM) ‡ (1999)	24	—	49	—	78	—	142	*M Gate and M and A ½*
(SC. 2.0)	19.7	27.8	39.4	53.2	71.9	97.1	131	
ASIC								
ASIC usable Mtransistors/cm^2 (auto layout) (1999)	20	28	40	54	73	99	133	*M Gate and M and A ½*
(SC. 2.0)	19.7	27.8	39.4	53.2	71.9	97.1	131	
ASIC max chip size at production (mm^2) (maximum lithographic field size) (1999)	800	800	800	800	800	800	800	*Lithographic Field Size*
(SC. 2.0)	800	800	800	800	572	572	572	
ASIC maximum functions per chip at production (Mtransistors/chip) (fit in maximum lithographic field size) (1999)	160	224	320	432	584	800	1064	*Market — Performance/ Timing*
(SC. 2.0)	157	223	315	426	411	556	751	

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 1j ***High-Performance MPU and ASIC*** *Product Generations and Chip Size Model—Long Term Years**

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]
Logic (Low-volume Microprocessor) High-performance ‡			
Generation at production ‡ (1999)/(SC. 2.0)	—	p11h	—
Functions per chip (million transistors) (1999)	2,494	7,053	19,949
(SC. 2.0)	1,381	3,907	11,052
Chip size at production (mm^2) § (1999)	713	817	937
(SC. 2.0)	427	489	561
High-performance MPU Mtransistors/cm^2 at production (including on-chip SRAM) ‡ (1999)	350	863	2,130
(SC. 2.0)	324	799	1,970
ASIC			
ASIC usable Mtransistors/cm^2 (auto layout) (1999)	328	811	2,000
(SC. 2.0)	324	799	1,970
ASIC maximum chip size at production (mm^2) (maximum lithographic field size) (1999)	800	800	800
(SC. 2.0)	572	572	572
ASIC maximum functions per chip at ramp (Mtransistors/chip) (fit in maximum lithographic field size) (1999)	2,624	6,488	16,000
(SC. 2.0)	1,852	4,568	11,269

Since only the 2011 odd-year product generation data column is available in the Long Term table format, interpolated numbers were calculated and included in the 2008 and 2014 node columns. The extended market-need-based product trends for the product generation two-year-cycle years (1999, 2001, 2003, 2005, 2007, 2009, 2011, 2013) are forecast to follow patterns established in Near Term Table 1a.

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

OTHER ORTC TABLES, TWG LINE ITEMS/OWNERS

Table	Line Item	TWG Owner
♦ Table 2a,b	Litho Field Size	Lithography
♦	Wafer Size	Front End Processes, Factory Integration
♦ Table 3a,b	# of Chip I/O's	Test, Design
♦	# of Package Pins/Balls	Test, Assembly & Packaging
♦ Table 4a,b	Chip Pad Pitch	Assembly & Packaging
♦	Cost-Per-Pin	Assembly & Packaging
♦ Table 4c,d	Chip Frequency	Design
♦	Chip-to-Board Freq.	Assembly & Packaging
♦	Max # Wire Levels	Interconnect
♦ Table 5a,b	Electrical Defects	Defect Reduction
♦ Table 6a,b	P.Supply Volt.	Process Integration, Devices, Structures
♦	Max. Power	Design, Process Integration, Devices, Structures
♦ Table 7a,b	Affordable Cost	Economic (Alan Allan acting)
♦	Test Cost	Test

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

*Table 2a ~~Chip-Size,~~ Lithographic-Field and Wafer-Size Trends—Near Term Years**

(Note: 1999 Lithographic field sizes represent current capability)

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005
Lithography Field Size							
Maximum lithographic field size — area (mm^2) (1999)	800	800	800	800	800	800	800
Lithography Field Size—area (mm^2) (SC. 2.0)	800	800	800	800	800	572	572
Maximum lithographic field size — length (mm) (1999)	32	32	32	32	32	32	32
Maximum lithographic field size — width (mm) (1999)	25	25	25	25	25	25	25
Lithographic field size (width X length [mm^2]) (SC. 2.0)	25x32	25x32	25x32	25x32	25x32	22x26	22x26
Maximum Substrate Diameter (mm) — High-volume Production (>20K wafer starts per month)							
Bulk or epitaxial or SOI wafer (1999)	200	200	300	300	300	300	300
(SC. 2.0)	200	200	300	300	300	300	300

*Table 2b ~~Chip-Size~~, Lithographic-Field and Wafer Size Trends—Long Term Years**

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]
Lithography Field Size			
Maximum lithographic field size—area (mm^2) (1999)	800	800	800
Lithography Field Size—area (mm^2) (SC. 2.0)	572	572	572
Maximum lithographic field size—length (mm) (1999)	32	32	32
Maximum lithographic field size—width (mm) (1999)	25	25	25
Lithographic field size (width X length [mm^2]) (SC. 2)	22x26	22x26	22x26
Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)			
Bulk or epitaxial or SOI wafer (1999)	300	300	450
(SC. 2.0)	300	450	450

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

*Table 3a Performance of Packaged Chips: Number of Pads and Pins—Near Term Years**

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90 nm	2005
Number of Chip I/Os (Number of Total Chip Pads) — Maximum							
Total pads—MPU (1999)	2,304	2,560	3,042	3,042	3,042	3,042	3,042
Signal I/O—MPU (1/3 of total pads) (1999)	768	1,024	1,024	1,024	1,024	1,024	1,024
Power and ground pads—MPU (2/3 of total pads) (1999)	1,536	1,536	2,018	2,018	2,018	2,018	2,018
Total pads—ASIC high-performance (1999)	1,400	1,800	2,200	2,600	3,000	3,400	3,800
Signal I/O pads—ASIC high-performance (½ of total pads) (1999)	700	900	1,100	1,300	1,500	1,700	1,900
Power and ground pads—ASIC high-performance (½ of total pads) (1999)	700	900	1,100	1,300	1,500	1,700	1,900
Chip-to-package pads (Peripheral) (1999)	368	397	429	464	501	541	584
Number of Total Package Pins/Balls—Maximum							
Microprocessor/controller, cost-performance (1999)	740	821	912	1,012	1,123	1,247	1,384
ASIC (high-performance) (1999)	1,600	1,792	2,007	2,248	2,518	2,820	3,158

*Table 3b Performance of Packaged Chips: Number of Pads and Pins—Long Term Years**

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 [60 nm]	2011 [40 nm]	2014 [30 nm]
Number of Chip I/Os (Number of Total Chip Pads)—Maximum			
Total pads—MPU (1999)	3,840	4,224	4,416
Signal I/O pads—MPU (1/3 of total pads) (1999)	1,280	1,408	1,472
Power and ground pads—MPU (2/3 of total pads) (1999)	2,560	2,816	2,944
Total pads—ASIC high-performance (1999)	4,600	5,400	6,000
Signal I/O pads—ASIC high-performance (½ of total pads) (1999)	2,300	2,700	3,000
Power and ground pads—ASIC high-performance (½ of total pads) (1999)	2,300	2,700	3,000
Chip-to-package pads (Peripheral) (1999)	736	927	1,167
Number of Total Package Pins/Balls—Maximum			
Microprocessor/controller, cost-performance (1999)	1,893	2,589	3,541
ASIC (high-performance) (1999)	4,437	6,234	8,758

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

*Table 4a Performance and Package Chips: Pads, Cost~~, and Frequency~~—Near Term Years**

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (Sc. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005
Chip Pad Pitch (micron)							
Pad pitch—ball bond (1999)	50	48	47	45	43	42	40
(2000)	50	50	45	35	30	25	20
Pad pitch—wedge bond (1999)	45	43	42	40	39	38	35
(2000)	45	45	40	35	30	25	20
Package cost (cents/pin) (cost-performance)—minimum (1999)	200	200	200	200	182	165	150
(2000)	200	200	175	175	150	150	130
Pad Pitch—area array (handheld, low-cost, harsh) NEW	180	165	150	130	120	110	100
Cost-Per-Pin							
Package cost (cents/pin) (cost-performance)—maximum (1999)	1.90	1.81	1.71	1.63	1.55	1.47	1.40
(2000)	1.90	1.40	1.33	1.26	1.20	1.14	1.08
Package cost (cents/pin) (cost-performance)—minimum (1999)/(2000)	0.90	0.86	0.81	0.77	0.73	0.70	0.66
Package cost (cents/pin) (Memory)—maximum (1999)/(2000)	1.90	1.71	1.54	1.39	1.25	1.12	1.01
Package cost (cents/pin) (Memory)—minimum (1999)/(2000)	0.40	0.38	0.36	0.34	0.33	0.31	0.29

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

*Table 4b Performance and Package Chips: Pads, Cost~~, and Frequency~~—Long Term Years**

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]
Chip Pad Pitch (micron)			
Pad pitch—ball bond (1999)	40	40	40
(2000)	20	20	20
Pad Pitch—wedge bond (1999)	35	35	35
(2000)	20	20	20
Pad Pitch—area array (cost-performance, high-performance) (1999)	150	150	150
(2000)	115	100	80
Pad Pitch—area array (handheld, low-cost, harsh) NEW	70	50	35
Cost-Per-Pin			
Package cost (cents/pin) (cost-performance)—maximum (1999)	1.20	1.03	0.88
(2000)	1.03	0.98	0.93
Package cost (cents/pin) (cost-performance)—minimum (1999)/(2000)	0.57	0.49	0.42
(1999)/(2000)	0.74	0.54	0.39
Package cost (cents/pin) (memory)—minimum (1999)/(2000)	0.25	0.22	0.19

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

*Table 4c Performance and Package Chips: ~~Pads, Cost, and~~ Frequency, On-Chip Wiring Levels—Near Term Years**

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90 nm	2005
Chip Frequency (MHz)							
On-chip local clock, (high-performance) (1999)	1,250	1,486	1,767	2,100	2,490	2,952	3,500
(2000)		1620	2,100	2,490	2,952	3,500	4,150
On-chip, across-chip clock (high-performance) (1999)	1,200	1,321	1,454	1,600	1,724	1,857	2,000
(2000)		1,386	1,600	1,724	1,857	2,000	2,155
On-chip, across-chip clock, high-performance ASIC (1999)	500	559	626	700	761	828	900
(2000)		592	700	761	828	900	980
On-chip, across-chip clock (cost-performance) (1999)	600	660	727	800	890	989	1,100
(2000)		693	800	890	989	1,100	1,225
Chip-to-board (off-chip) speed (high-performance, reduced-width, multiplexed bus) (1999)	1,200	1,321	1,454	1,600	1,724	1,857	2,000
(2000)		1386	1,600	1,724	1,857	2,000	2,155
Chip-to-board (off-chip) speed (high-performance, for peripheral buses) (1999)	480	589	722	885	932	982	1,035
(2000)	480	693	800	862	929	1000	1078
Maximum number wiring levels—maximum (1999)/(2000)	7	7	7	8	8	8	9
Maximum number wiring levels—minimum (1999)/(2000)	6	6	7	7	8	8	8

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 4d Performance and Package Chips: ~~Pads, Cost, and~~ Frequency,
On-Chip Wiring Levels *—Long Term Years**

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)		2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)		2008 [60 NM]	2011 [40 NM]	2014 [30 NM]
Chip Frequency (MHz)				
On-chip local clock, (high-performance)	(1999)	6,000	10,000	13,500
	(2000)	7,115	11,050	14,920
On-chip, across-chip clock (high-performance)	(1999)	2,500	3,000	3,600
	(2000)	2,655	3,190	3,825
On-chip, across-chip clock (high-performance ASIC)	(1999)	1,200	1,500	1,800
	(2000)	1,295	1,595	1,913
On-chip, across-chip clock (cost-performance)	(1999)	1,400	1,800	2,200
	(2000)	1,522	1,925	2,350
Chip-to-board (off-chip) speed (high-performance, reduced-width, multiplexed bus)	(1999)	2,500	3,000	3,600
	(2000)	2,655	3,190	3,825
Chip-to-board (off-chip) speed (high-performance, for peripheral buses)	(1999)	1,285	1,540	1,800
	(2000)	1328	1595	1913
Maximum number wiring levels—minimum	(1999)/(2000)	9	10	10
Maximum number wiring levels—minimum	(1999)/(2000)	9	9	10

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

*Table 5a Electrical Defects—Near Term Years**

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005
Defect Reduction							
DRAM at production electrical D_0 chip size at 85% yield (d/m^2) § (1999)	1,249	1,193	1,140	1,089	1,040	994	950
(2000)	1,259	1,282	1,302	1,170	1,050	942	1126
MPU at production electrical D_0 chip size at 75% yield (d/m^2) §§ (1999)	1,742	1,742	1,742	1,552	1,383	1,321	1,262
(2000)	1,742	1,742	1,742	1,664	1,590	1,519	1,452
ASIC first year electrical D_0 at 65% yield (d/m^2) (1999)	562	562	562	562	562	562	562
(2000)	562	562	562	562	787	787	787
Minimum, mask count—maximum (1999)	24	24	24	24	25	25	26
(2000)	24	24	24	25	25	26	26
Minimum, mask count—minimum (1999)	22	23	23	24	24	24	24
(2000)	22	23	24	24	24	24	24

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

*Table 5b Electrical Defects—Long Term Years**

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]
Defect Reduction			
DRAM at production electrical D_0 chip size at 85% yield (d/m^2) § (1999)	828	723	630
(2000)	807	865	660
MPU at production electrical D_0 chip size at 75% yield (d/m^2) §§ (1999)	1,101	960	837
(2000)	1,266	1,104	963
ASIC first year electrical D_0 at 65% yield (d/m^2) (1999)	562	562	562
(2000)	787	787	787
Minimum, mask count—maximum (1999)	28	28	30
(2000)	28	28	30
Minimum, mask count—minimum (1999)	26	28	29
(2000)	26	28	29

D_0—defect density

§ DRAM Model—Cell Factor (design/process improvement) targets are: 1999-2004/8x; 2005-2010/6x; 2011-2016/4x. DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except: 1) at the Introduction phase, after the 8Gbit interim generation, the introduction rate is 4x/5years (2x/2-3yrs); and 2) at the Production phase, after the interim 32Gbit generation, the introduction rate is 4x/5years (2x/2-3yrs). InTER-generation chip size growth rate varies to maintain 1 chip per 572mm^2 field at Introduction and 2 chip per 572mm^2 field at Production. The more aggressive "best case opportunity" technology node trends allow the Production-phase products to remain at 2x bits/chip every 2 years and still fit within the target of two DRAM chips per 572mm^2 field size, through the 32Gbit interim generation. The InTRA-generation chip size shrink model is 0.5× every technology node in-between cell factor reductions.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates can be kept flat through 2001, due to the more aggressive MPU/ASIC half-pitch technology node trend; but beyond 2001, the target growth rate is 1.2× growth every four years. The InTRA-generation chip size shrink model is 0.5× every two years through 2001, then 0.5× every three years after 2001.

* In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

*Table 6a Power Supply and Power Dissipation—Near Term Years**

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005
Power Supply Voltage (V)							
Minimum logic V_{dd} (V)—maximum (for maximum performance) (1999)	1.8	1.8	1.5	1.5	1.5	1.2	1.2
(2000)	1.8	1.8	1.5	1.5	1.2	1.2	1.1
Minimum logic V_{dd} (V)—minimum (for lowest power) 1999)	1.5	1.5	1.2	1.2	1.2	0.9	0.9
(2000)	1.5	1.5	1.2	1.2	0.9	0.9	0.8
Maximum Power							
High-performance with heatsink (W)	90	100	115	130	140	150	160
(2000)	90	108	130	140	150	160	170
Battery (W)—(hand-held) (1999)	1.4	1.6	1.7	2.0	2.1	2.3	2.4
(2000)	1.4	1.7	2.0	2.1	2.3	2.4	2.6

*Table 6b Power Supply and Power Dissipation—Long Term Years**

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]
Power Supply Voltage (V)			
Minimum logic V_{dd} (V)—maximum (for maximum performance) (1999)	0.9	0.6	0.60
(2000)	0.9	0.6	0.60
Minimum logic V_{dd} (V)—minimum (for lowest power) (1999)	0.6	0.5	0.30
(2000)	0.6	0.5	0.30
Maximum Power			
High-performance with heatsink (W) (1999)	170	174	183
(2000)	171	177	186
Battery (W)—(hand-held) (1999)	2.0	2.2	2.4
(2000)	2.1	2.3	2.5

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

*Table 7a Cost—Near Term Years**

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005
Affordable Cost per Function ++							
DRAM cost/bit at (packaged microcents) at samples/introduction (1999)/(SC. 2.0)	42	—	21	—	11	—	5.3
DRAM cost/bit at (packaged microcents) at production § (1999)/(SC. 2.0)	15	—	7.6	—	3.8	—	1.9
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§ (1999)/(SC. 2.0)	1,735	—	868	—	434	—	217
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§ (1999)/(SC. 2.0)	1,050	—	525	—	262	—	131
High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§ (1999)/(SC. 2.0)	245	—	123	—	61	—	31
Cost-Per-Pin (see Table 4) (1999)/(SC. 2.0)	—	—	—	—	—	—	—
Test							
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—maximum (1999)/(SC. 2.0)	8	7	7	6	6	5	5
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—minimum (1999)/(SC. 2.0)	4	3	3	3	3	2	2
Volume tester cost/pin ($K/pin) (cost-performance MPU) (1999)/(SC. 2.0)	8	8	7	7	6	6	5

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

*Table 7b Cost—Long Term Years**

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]
Affordable Cost per Function ++			
DRAM cost/bit (packaged microcents) at samples/introduction (1999)/(SC. 2.0)	—	0.66	—
DRAM cost/bit (packaged microcents) at production § (1999)/(SC. 2.0)	—	0.24	—
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§ (1999)/(SC. 2.0)	—	27	—
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§ (1999)/(SC. 2.0)	—	16	—
High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§ (1999)/(SC. 2.0)	—	3.8	—
Cost-Per-Pin (see Table 4) (1999)/(SC. 2.0)	—	—	—
Test			
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—maximum (1999)/(SC. 2.0)	5	5	5
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—minimum (1999)/(SC. 2.0)	N/A	N/A	N/A
Volume tester cost/pin ($K/pin) (cost-performance MPU) (1999)/(SC. 2.0)	4	2	2

++ *Affordable packaged unit cost per function based upon Average Selling Prices (ASPs) available from various analyst reports less Gross Profit Margins (GPMs); 35% GPM used for commodity DRAMs and 60% GPM used for MPUs; 0.5×/two years inTER-generation reduction rate model used; .55×/year inTRA-generation reduction rate model used; DRAM unit volume life-cycle peak occurs when inTRA-generation cost per function is crossed by next generation, typically 7–8 years after introduction; MPU unit volume life-cycle peak occurs typically after four years, when the next generation processor enters its ramp phase (typically two years after introduction).*

§ *DRAM Model—**Cell Factor (design/process improvement) targets are: 1999-2004/8x; 2005-2010/6x; 2011-2016/4x. DRAM product** generations **are usually increased by** 4× bits/chip every four years with interim 2× bits/chip generations, **except: 1) at the Introduction phase, after the 8Gbit interim generation, the introduction rate is 4x/5years (2x/2-3yrs); and 2) at the Production phase, after the interim 32Gbit generation, the introduction rate is 4x/5years (2x/2-3yrs).** InTER-generation chip size growth rate **varies to maintain 1 chip per 572mm^2 field at Introduction and 2 chip per 572mm^2 field at Production. The more aggressive "best case opportunity" technology node trends allow the Production-phase products to remain at 2x bits/chip every 2 years and still fit within the target of two DRAM chips per 572mm^2 field size, through the 32Gbit interim generation.** The InTRA-generation chip size shrink model is 0.5× **every technology node in-between cell factor reductions.***

§§ *MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates **can be kept flat through 2001, due to the more aggressive MPU/ASIC half-pitch technology node trend**; but beyond 2001, the target growth rate is 1.2× growth every four years. The InTRA-generation chip size shrink model is 0.5× every two years through 2001, then 0.5× every three years after 2001.*

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

ITRS TABLE DEFINITIONS/GUIDELINES

Proposal Rev1, 7/11/00

- Technology Requirements Perspective
  - Near-Term Years : First Yr. Ref.+ 6 yrs F'cast (ex. 1999 through 2005), annually
  - Long-Term Years : Following 9 years (ex.: 2008, 2011, and 2014), every 3 years
- Technology Node :
  - General indices of technology development.
  - Approximately 70% of the preceding node, 50% of 2 preceding nodes.
  - Each step represents the creation of significant technology progress
  - Example: DRAM half pitches (2000 ITRS) of 180, 130, 90, 65, 45 and 33nm

  *Year 2000 : Smallest 1/2 pitch among DRAM, ASIC, MPU, etc
- Year of Production:
  - The volume = *10K units (devices)/month. ASICs manufactured by same process technology are granted as same devices
  - Beginning of manufacturing by *a company and another company starts production within 3 months
- Technology Requirements Color:
  - Red : Manufacturable Solutions are NOT known
  - Yellow : Manufacturable Solutions are known
  - White : Manufacturable Solutions exist, and they are being optimized

  *Year 2000 : Red cannot exist in next 3 years (2000, 2001, 2002)**

  *Year 2000 : Yellow cannot exist in next 1 year (2000)

** *Exception: Solution NOT known, but does not prevent Production manufacturing*

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

GLOSSARY – ORTC 2000 UPDATE EDITION

KEY ROADMAP TECHNOLOGY CHARACTERISTICS TERMINOLOGY (WITH OBSERVATIONS AND ANALYSIS)

CHARACTERISTICS OF MAJOR MARKETS

TECHNOLOGY NODE (nm)—

Each technology node step represents the creation of significant technology progress - approximately 70% of the preceding node, 50% of 2 preceding nodes. Example: DRAM half pitches (2000 ITRS) of 180, 130, 90, 65, 45 and 33 nm. The ground rules of process governed by the smallest feature printed. The half-pitch of first-level interconnect dense lines is most representative of the DRAM technology level required for the smallest economical chip size. For logic, such as microprocessors (MPUs), physical bottom gate length is most representative of the leading-edge technology level required for maximum performance. MPU and ASIC logic interconnect half-pitch processing requirement typically refers to the first metal layer and lags behind DRAM half-pitch, which may refer either first layer polysilicon or metal. For cost reasons, high-volume, low-cost ASIC gate-length requirements will typically match DRAM half-pitch targets, but the low-volume leading-edge high-performance ASIC gate-length requirements will track closely with MPUs.

"MOORE'S LAW"—An historical observation by Intel executive, Gordon Moore, that the market demand (and semiconductor industry response) for functionality per chip (bits, transistors) doubles every 1.5 to 2 years. He also observed that MPU performance [clock frequency (MHz) × instructions per clock = millions of instructions per second (MIPS)] also doubles every 1.5 to 2 years. Although viewed by some as a "self-fulfilling" prophecy, "Moore's Law" has been a consistent macro trend, and key indicator of successful leading-edge semiconductor products and companies, for the past 30 years.

"COST-PER-FUNCTION" MANUFACTURING PRODUCTIVITY IMPROVEMENT DRIVER—In addition to "Moore's Law", there is a historically-based "corollary" to the "law," which suggests that, to be competitive, manufacturing productivity improvements must also enable the cost-per-function (microcents per bit or transistor) to decrease by -29% per year. Historically, when functionality doubled every 1.5 years, then cost-per-chip (packaged unit) could double every six years and still meet the cost-per-function reduction requirement. If functionality doubles only every two years, as suggested by consensus DRAM and MPU models of the 1999 ITRS, then the manufacturing cost per chip (packaged unit) must remain flat.

"Affordable" Packaged Unit Cost/Function—Final cost in microcents of the cost of a tested and packaged chip divided by ***Functions/Chip.*** Affordable costs are calculated from historical trends of affordable average selling prices [gross annual revenues of a specific product generation divided by the annual unit shipments] less an estimated gross profit margin of approximately 35% for DRAMs and 60% for MPUs. The affordability per function is a guideline of future market "tops-down" needs, and as such, was generated independently from the chip size and function density. Affordability requirements are expected to be achieved through combinations of—1) smaller chip sizes from technology and design improvements; 2) increasing wafer diameters; 3) decreasing equipment cost-of-ownership (CoO); 4) increasing equipment overall equipment effectiveness; 5) reduced package and test costs; 6) improved design tool productivity; and 7) enhanced product architecture and integration.

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

DRAM Generation* at *(product generation life-cycle level)—The anticipated bits/chip of the DRAM product generation introduced in a given year, manufacturing technology capability, and life-cycle maturity (Demonstration, Introduction, Sample, Production, Ramp, Peak).

MPU Generation* at (*product generation life-cycle level)—The generic processor generation identifier for the anticipated Microprocessor Unit (MPU) product generation functionality (logic plus SRAM transistors per chip) introduced in a given year, manufacturing technology capability, and life-cycle maturity (Introduction, Ramp, Peak, Embedded).

Cost-Performance MPU—MPU product optimized for lowest cost by minimizing on-chip SRAM to level-one (L1) cache only (32Kbytes/1999). Logic functionality and L1 cache typically double every 2-year generation. This typically has a 6-year (introduction plus ramp plus peak) computer-market-application life-cycle before being replaced by the next generation cost-performance MPU, then continues on in embedded applications.

High-performance MPU—MPU product optimized for maximum system performance by using a shrunk cost-performance ramp-level MPU core combined with a large (1Mbyte/1999) level-two (L2) SRAM. Logic functionality and L2 cache typically double every two-year generation. Typically has only a 4-year (ramp and peak) life cycle in the relatively low-volume, higher-priced, high-performance computer market. There is no classic "embedded" application for the high-SRAM-content MPU, but that may change as future market demand develops for multiple-MPU-per box internet server and communication processor applications emerge. Those applications will provide increased demand for more cost-effective inTRA generation shrinks of the high-performance MPU, thus extending the life-cycles of future generations.

PRODUCT INTER-GENERATION—Product generation-to-generation targets for periodically increasing on-chip functionality and allowable chip size. The targets are set to maintain "Moore's Law," while preserving economical manufacturability. The 1999 ITRS consensus target for the rate of increase of DRAM and MPU inTER-generation functionality is 2×/chip every two years. The allowable inTER-generational chip size growth for DRAMs was 1.2× every four years in the 1999 ITRS, but is now limited by the maximum available lithography field size and also the cell shrink limitations imposed by the achievable cell area factor targets . For MPUs, the allowable chip size growth is flat through 2001, then grows at 1.2× every four years. To add only 20% in area every four years, while quadrupling functionality, requires an inTER-generation design productivity which further reduces chip size by an additional minus 7–8 % per year. This design-related productivity reduction is in addition to the basic lithography-provided area reduction of -11% per year.

PRODUCT INTRA-GENERATION—Within a given product generation. The consensus-based targets reduce chip size (by shrinks and "cut-downs") utilizing the latest available manufacturing and design technology at every point through the roadmap. The ITRS consensus targets for both DRAM and MPU reduce chip size within a generation by minus 50% per technology node. For DRAM, this reduction of minus 50% occurs every three years, or minus 37% every two years. For MPU, the 50% reduction occurs every two years through 2001, then slows to minus 37% per two years (same as DRAM).

YEAR OF DEMONSTRATION—Year in which the leading chip manufacturer supplies an operational sample of a product as a demonstration of design and/or technology node processing feasibility and prowess. A typical venue for the demonstration is a major semiconductor industry conference, such as the International Solid State Circuits Conference (ISSCC) held by the Institute of Electrical and Electronic Engineers (IEEE). Demonstration samples are typically manufactured with early development or demonstration- level manufacturing tools and processes. Historically, DRAM products have been demonstrated at 4× bits-per-chip every three years at the leading-edge process technology node, typically 2–3 years in advance of actual market introduction. DRAM demonstration chip sizes have doubled every six years, requiring an increasing number of shrinks and delay before market introduction is economically feasible. Frequently, chip sizes are larger than the field sizes available from lithography equipment, and must be "stitched" together via multiple-exposure

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

techniques that are feasible only for very small quantities of laboratory samples.
Example: 1997/ISSCC/1Gb DRAM.

YEAR OF INTRODUCTION (DRAM)—Year in which the leading chip manufacturer supplies small quantities of engineering samples (<1K). These are provided to key customers for early evaluation, and are manufactured with qualified production tooling and processes. To balance market timeliness and economical manufacturing, DRAM products will be introduced at 2× functionality per chip every two years. In addition, manufacturers will delay introduction until a chip-size shrink or "cut-down" level is achieved which limits the inTER-generation chip-size growth to 1.2× every 4 years, or approximately 1.1× every 2-year generation **in the 1999 ITRS, but is now limited by the maximum available lithography field size and also the cell shrink limitations imposed by the achievable cell area factor targets** Example: 1999/1Gb DRAM.

YEAR OF PRODUCTION (DRAM)—Year in which leading chip manufacturers begin shipping volume quantities (**10K/month**) of product manufactured with qualified production tooling and processes **and is followed within three months by a second manufacturer**. This product typically contains one-fourth (1/4) the bits per chip of the introduction-level generation design, from which it is "cut-down." Example: 1999/256Mb DRAM.

YEAR OF INTRODUCTION (MPU)—Year in which the leading chip manufacturer supplies small quantities of engineering samples (<1K). These are provided to key customers for early evaluation, and are manufactured with qualified production tooling and processes. The introduction cost-performance MPU may be combined in a multi-chip module, along with L2 cache, in low-volume computer applications which demand high performance.

YEAR OF PRODUCTION (MPU)— Year in which leading chip manufacturers begin shipping volume quantities (**10K/month**) of product manufactured with qualified production tooling and processes **and is followed within three months by a second manufacturer**. As demand increases, the tooling and processes are being quickly "copied" into multiple modules of manufacturing capacity. Lower-volume, high-performance MPUs are also ramping concurrently as its co-existing cost-performance MPU core, but the L2 cache is now included on-chip but with twice the memory as its high-performance-generation predecessor.

Functions/Chip—The number of bits (DRAMs) or logic transistors (MPUs, application-specific integrated circuits [ASICs]) that can be cost-effectively manufactured on a single monolithic chip at the available technology level. Logic functionality (transistors per chip) include both SRAM and logic transistors. DRAM functionality (bits per chip) is based only on the bits (after repair) on a single monolithic chip.

Chip Size (mm^2)—The typical area of the monolithic memory and logic chip that can be affordably manufactured in a given year based upon the best available leading-edge design and manufacturing process. (Estimates are projected based upon historical data trends and the ITRS analyst consensus models).

Functions/cm^2—The density of functions in a given square centimeter = ***Functions/Chip*** on a single monolithic chip divided by the ***Chip Size***. This is an average of the density of all of the functionality on the chip, including pad area and wafer scribe area. In the case of DRAM, it includes the average of the high-density cell array and the less-dense peripheral drive circuitry. In the case of the MPU products, it includes the average of the high-density SRAM and the less-dense random logic. In the case of ASIC, it will include high-density embedded memory arrays, averaged with less dense array logic gates and functional cores. Most typical ASIC designs will be slightly less dense than the high-performance MPUs, which are mostly SRAM.

DRAM Cell Array Area Percentage—The maximum practical percentage of the total DRAM chip area that the cell array can occupy at the various stages of the generation life cycle. At the introduction chip size targets, this percentage must be typically less than 70% to allow space for the peripheral circuitry, pads, and wafer scribe area. Since the pads and scribe

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

area do not scale with lithography, the maximum cell array percentage is reduced in other inTRA-generation shrink levels (typically less than 55% at the production level, and less than 50% at the ramp level).

DRAM Cell Area (µm²)—The measure of the maximum allowable DRAM memory bit cell area specified by the requirement to meet the target chip size and cell array area percentage requirements. May also be expressed as the cell area factor – number of equivalent units of area of a square of the DRAM half-pitch. Minimizing the area for the cell is in conflict with the desire to maximize the capacitance storage capability of the continuously shrinking cell. This creates a conflict between the technical feasibility of the cell area required to meet the economic constraints of the maximum allowable chip size.

DRAM Cell Area Factor—The measure of the maximum allowable DRAM memory bit cell area, expressed as the number of equivalent units of area of a square of the DRAM half-pitch.

Example: 1999: square of the half-pitch = $(180\ nm)^2 = .032\ \mu m^2$; maximum cell area for 1Gb DRAM to be < 70% of total chip area = $0.26\ \mu m^2$; therefore, the maximum cell area factor = 0.26/0.32 = 8. The cell factor is also often expressed by equivalent aspect ratios of the half-pitch units (2×4 = 8, 2×3 = 6, 2×2=4, 1.6×1.6=2.5, etc.).

Usable Transistors/cm² (High-performance ASIC, Auto Layout)—Number of transistors per cm^2 designed by automated layout tools for highly differentiated applications produced in low volumes. High-performance, leading-edge, embedded-array ASICs include both on-chip array logic cells, as well as dense functional cells (MPU, I/O, SRAM, etc). Density calculations include the connected (useable) transistors of the array logic cells, in addition to all of the transistors in the dense functional cells. The largest high-performance ASIC designs will fill the available production lithography field.

CHIP AND PACKAGE—PHYSICAL AND ELECTRICAL ATTRIBUTES

Number of Chip I/Os – Total (Array) Pads—The maximum number of chip signal I/O pads plus power and ground pads permanently connected to package plane for functional or test purposes, or to provide power/ground contacts (including signal conditioning). These include any direct chip-to-chip interconnections or direct chip attach connections to the board (Package plane is defined as any interconnect plane, leadframe, or other wiring technology inside a package, i.e., any wiring that is not on the chip or on the board.). MPUs typically have a ratio of signal I/O pads to power/ground pads of 1:2, whereas the high-performance ASIC ratio is typically 1:1.

Number of Chip I/Os – Total (Peripheral) Pads—The maximum number of chip signal I/O plus power and ground pads for products with contacts only around the edge of a chip.

Pad Pitch—The distance, center-to-center, between pads, whether on the peripheral edge of a chip, or in an array of pads across the chip.

Number of Package Pins/Balls—The number of pins or solder balls presented by the package for connection to the board (may be fewer than the number of chip-to-package pads because of internal power and ground planes on the package plane or multiple chips per package).

Package cost (cost-performance)—Cost of package envelope and external I/O connections (pins/balls) in cents/pin.

Chip Frequency (MHz)

On-chip, local clock, high-performance—On-chip clock frequency of high-performance, lower volume microprocessors in localized portions of the chip.

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

On-chip, across-chip clock—On-chip clock frequency of microprocessors and ASICs for interconnect signals that run across the full width of the chip (Typically, this is lower than the localized clock performance due to capacitance loading of the long cross-chip interconnect.).

Chip-to-board (off-chip) speed (high-performance, reduced-width, multiplexed bus)—Maximum signal I/O frequency to specialized board reduced-width, multiplexed buses.

Chip-to-board (off-chip) speed (high-performance, peripheral buses)—Maximum signal I/O frequency to board peripheral buses of high and low volume logic devices.

Other Attributes

Lithographic Field Size (mm^2)—Maximum single step or step-and-scan exposure area of a lithographic tool at the given technology node. **The specification represents the mimimum specification that a semiconductor manufacturer might specify for a given technology node. The maximum field size may be specified higher than the ORTC target values, and the final exposure area may be achieved by various combinations of exposure width and scan length.**

Maximum Number Of Wiring Levels—On-chip interconnect levels including local interconnect, local and global routing, power and ground connections, and clock distribution.

FABRICATION ATTRIBUTES AND METHODS

Electrical D_0 Defect Density (d/m^{-2})—Number of electrically significant defects per square meter at the given technology node, production life-cycle year, and target probe yield.

Minimum Mask Count—Number of masking levels for mature production process flow with maximum wiring level (Logic).

MAXIMUM SUBSTRATE DIAMETER (MM)

Bulk or Epitaxial or Silicon-on-Insulator Wafer—Silicon wafer diameter used in volume quantities by mainstream IC suppliers. The ITRS timing targets, contributed by the Factory Integration Technology Working Group, are based on the first 20K wafer-starts-per-month manufacturing facility, versus the first-pilot-line timing target of the 1997 NTRS.

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

ELECTRICAL DESIGN AND TEST METRICS

Power Supply Voltage (V)

Minimum Logic V_{dd}— Nominal operating voltage of chips from power source for operation at design requirements.

Maximum Power

High-performance with heat sink (W)—Maximum total power dissipated in high-performance chips with an external heat sink.

Battery (W)—Maximum total power/chip dissipated in battery operated chips.

DESIGN AND TEST

Volume Tester Cost/Pin ($K/pin)—Cost of functional (chip sort) test in high volume applications divided by number of package pins.

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.